Modeling of Open Defects in CMOS Integrated Circuits and Test Techniques for Submicron Technologies

by

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Summary

Since the 80s, the electronic field had been supported in the silicon transistor. The technological advances had made possible to have smaller transistors because lithography and the fabrication process have been improved. As a consequence the density integration and the complexity of the circuits have been increased. In the new advanced technologies opens have became an important defect contributor. Because this, it is very important the study of these defects and to determine the optimal exciting conditions for testing them.

This thesis has the following organization:

In Chapter 1, mechanisms producing open defects are described. Some important fault models are reviewed. Then, different test methodologies are introduced. Logic test, delay testing and I_{DDQ} testing methodologies are introduced. Finally, previous work for open defects is reviewed.

In Chapter 2, the detectability of full opens in interconnections is investigated. A coupling model taking into account technology and topology parameters is proposed. The influence of the coupled signals to the floating one is investigated. Cases of full controllability, partial controllability and low controllability are considered. The effect of unsensitized gates is also investigated.

In Chapter 3, the behavior and detectability conditions of resistive opens in memory structures have been investigated. A symmetrical and a transmission gate based latches have been considered. The effect of initial voltage conditions prior to the application of the test vectors are investigated. Also charge sharing

effects affecting some open locations are analyzed. DFT testable latches have been proposed for detecting open defects located in undetectable branches. The results have been extended to flip-flop structures and a scan path chain. Timing conditions for detecting opens in a scan path chain are determined.

In Chapter 4, a new test technique for verifying time critical digital signals is proposed. The technique is based in analyzing the X-Y curves of the defective and non-defective signals. A compact and fast BIST circuitry based on a floating gate weighted adder comparator is proposed. The method has been successfully applied to detect delay violations due to crosstalk.

In Chapter 5, the conclusions of the work are given.

Sumario

El campo de la electrónica ha estado cimentado en el transistor de silicio desde los años ochentas. Transistores cada vez mas pequeños han sido posibles debido al avance de la electrónica en la litografía y los procesos de fabricación. Como consecuencia, se ha incrementado la densidad de integración y la complejidad de los circuitos integrados. En las nuevas tecnologías, los abiertos se han convertido en una fuente importante de defectos. Es debido a esto que es importante estudiar estos defectos y determinar sus condiciones óptimas de excitación.

La organización de esta tesis es la siguiente:

Algunos mecanismos que producen los abiertos y algunos modelos de falla importantes son descritos en el capitulo 1. Después diferentes metodologías de prueba son revisadas. Metodologías de prueba lógica, prueba de retardo y prueba I_{DDQ} son introducidas. Finalmente se revisan los trabajos previos para defectos de abiertos.

En el capitulo 2 se investiga la detectabilidad de abiertos totales en interconexiones. Se propone un modelo de acoplamiento el cual toma en cuenta la tecnología y los parámetros tecnológicos. Se investiga la influencia de las señales acopladas a una señal flotante. Se consideran los casos de controlabilidad total, controlabilidad parcial y baja controlabilidad. También se investiga el efecto de compuertas no sensibilizadas.

En el capitulo 3 se investiga el comportamiento y las condiciones de detectabilidad de abiertos resistivos en estructuras de memoria. Se ha considerado latches

simétricos y de compuertas de transmisión y los efectos de los voltajes de condiciones iniciales anteriores a la aplicación de los vectores de prueba. También se ha analizado los efectos de redistribución de carga para algunas localizaciones de abiertos. Se proponen latches detectables DFT para detectar defectos de abiertos localizados en ramas no detectables. Estos resultados son extendidos a estructuras de flip-flop y cadenas de scan path. También se determinan las condiciones de sincronización para detectar abiertos en una cadena scan path.

En el capitulo 4 se propone una nueva técnica para verificación del tiempo en señales digitales críticas. La técnica esta basada en el análisis de las curvas X-Y de señales defectuosas y no defectuosas. Se propone un circuito BIST rápido y compacto el cual esta basado en un comparador de compuertas flotantes. Esta técnica se ha probado exitosamente en la detección de violaciones de retardo debido a acoplos capacitivos.

Finalmente en el capitulo 5 se muestran las conclusiones de este trabajo.

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Por que no merezco todo el apoyado que me han dado por todo este tiempo

a mis demás familares

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Contents

Preface

Significant improvements in technologies and design of Integrated Circuits have been made since the first transistor was invented in the 40's decade. As transistor is moving deeper into the submicron technologies, its related parameters are scaling down. Among these, it can be mentioned the field oxide, threshold voltages, power supply, metals geometries and others. As a consequence of scaling the complexity and speed of integrated circuits is increasing. Modern integrated circuits in submicron technologies have million of transistors. Even more the number of vias/contacts exceeds the number of transistors. Hence, there is an important probability of a defective via/contact to occur. The use of new technologies like copper for the interconnections increases the likelihood of opens and malformed vias to occur respect to older technologies. Actually there is a great interest in modeling and testing methodologies for open defects. It has been found that this type of defect is an important contributor to test escapes.

In this work modeling and testability of open defects is addressed. The testability of full opens by I_{DDQ} and logic testing is investigated for CMOS combinational circuits. Using a proposed capacitance model simple analytical expressions are developed. These expressions are used to determine the testability of full opens. It is considered the influence of the circuit topology on the detectability of the open. The testability of resistive opens in CMOS memory elements by logic and delay testing is investigated. It is considered the effect of initial conditions for high resistive opens. DFT CMOS testable memory elements have been proposed in order to make detectable otherwise undetectable opens. The testing conditions for a scan path chain in the presence of open have been determined. A new technique for the verification of time digital critical signals is proposed.

This proposal is based in defined X-Y zone curves. An implementation of the technique is suggested. Floating gate transistors are used. The feasibility of the proposed technique to test delay violations due to crosstalk is explored.

Acronyms

ACS	After Clock Signal.
Al	Aluminum.
BCS	Before Clock Signal.
BIST	Built In Self Test.
CIS	Clocked Inverter Stage.
CMOS	Complementary Metal Oxide Semiconductor.
CMS	Closing Memory Stage.
CUT	Circuit Under Test.
DET	Detectable.
DFT	Design For Testability.
DS	Driver Stage.
FF	Flip-Flop.
FG	Floating Gates.
IC	Integrated Circuit.
I_{DDQ}	Quiescent Current Consumption.
INVS	Inverter Stage.
IS	Input Stage.
LT	Logic Testable.
NLT	Non-Logic Testable.
OS	Output Stage.
SA	Stuck-at.
SRAM	Static Random Access Memory.
TG	Transmission Gate.
t_{su}	Set-up Time.

Chapter 1

Introduction.

1.1 Manufacturing open defects

Since the 80s, the electronic field had been supported in the silicon transistor. The technological advances had made possible to have smaller transistors because lithography and the fabrication process have been improved. As a consequence the density integration and the complexity of the circuits have been increased. However several types of defects can appear due to alterations in the fabrication process. Defects can affect the functionability in integrated circuits (ICs). According with its impact, defects can be classified as parametric and catastrophic [1]. The impact of parametric defects can be global affecting to the entire IC or local affecting a small area of the IC. There is a widely spread of causes that provoke parametric defects among them we can mention: temperature gradient variations in the etching process, local aberrations in the lents, variation in the doping process. These defects can have a significant impact in analog circuits. Their effect in digital circuits is less severe. However, as the technology scale, their effects are becoming more important. Catastrophic defects affect the functionability of ICs as permanent, intermittent or transient faults. Permanent faults can be result of short circuits, open defects, gate-oxide short and other defects. Intermittent faults are those excited by a non zero probability. Transient faults are due to random events as alpha particles or noise phenomenon like crosstalk or groundbounce.

This thesis is mainly focused in open defects. Full-opens and partial opens (resistive opens) are considered. A full-open is when there is non influence from the input signal on the floating line (Figure 1.1). A resistive open is when the conductive material is not completely broken (Figure 1.1). As a consequence the resistance in this conducting path increases. Contacts/vias are a likely place for an open to occur [2] [3] [4] [5]. In actual technologies there are a high number of vias because the many metal levels [3] [4]. In Figure 1.2, breaks on vias are illustrated.

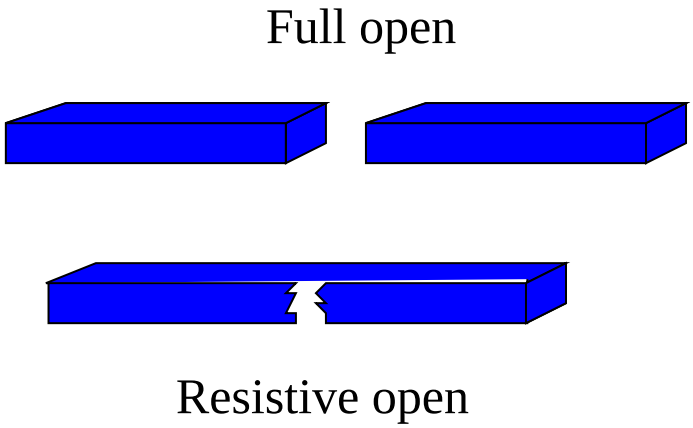


Figure 1.1: The concept of full and resistive open in interconnection lines.

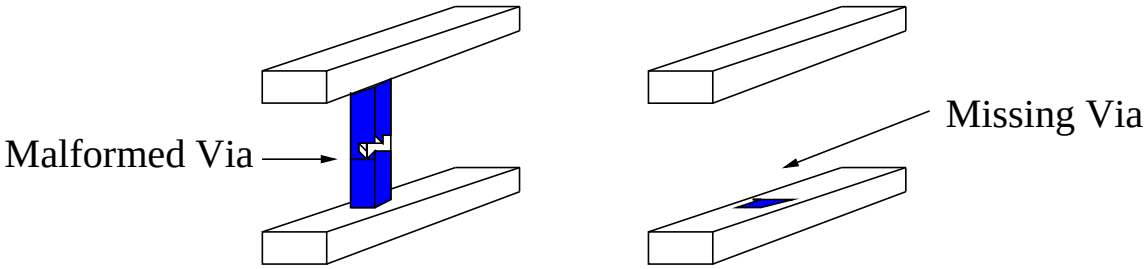


Figure 1.2: The concept of full open and resistive open in vias.

Poly and metal wires leaves hills in the oxide in planarization technologies [6] [7]. The bumps in the oxide can be smoothed by different chemical or mechanical methods. Due to this step coverage problems can occur. Which can produce

breaks in subsequent metallization layers.

Interconnection points between metals (via) or interconnection points between active area and metal/poly (contact) are likely points for full opens and resistive opens. A malformed contact or a via can give as result a defective connection. In subtractive-aluminum based technologies these problems became severe for 0.25μm generation and lower [8]. In cupper based technologies more defective connections are expected because integration capacity and metal levels have been increased. Damascene-copper process uses a dual-damascene process [9] [10]. In this case vias and metal lines are both patterned and etched prior to the additive metallization. In the flow of this process there is the potential for residual resist or polymer blockage in the damascene through metal or via [8]. Because this micromasking during the subsequent lithography step or blockage of the post-RIE metalization can occur. In Figure 1.3, a particle dust producing a resistive open in a copper based interconnection process is illustrated. The open defect density in copper shows a higher value that those opens in aluminum [8]. Higher metal levels are more prone to opens that those in lower metal levels.

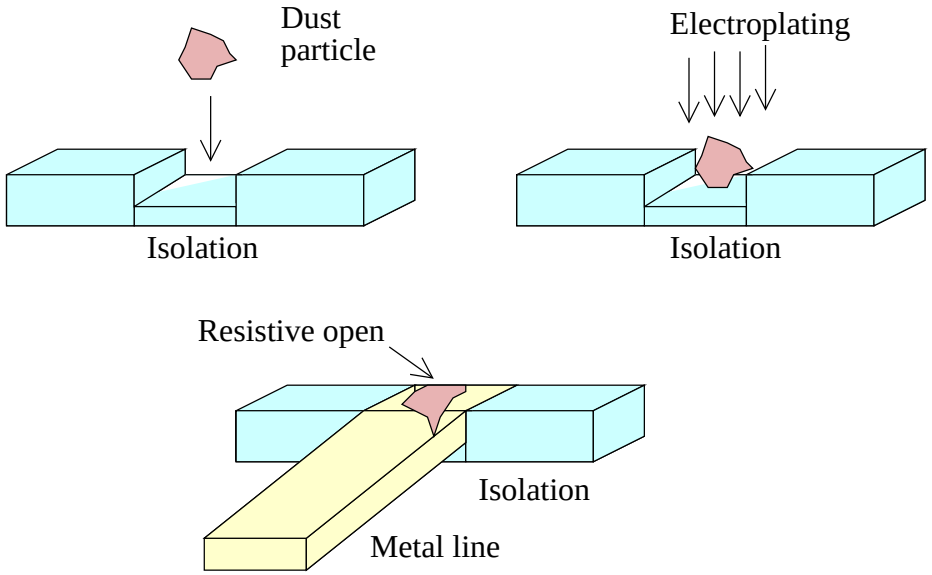


Figure 1.3: Resistive open in cupper process.

Other sources of opens are:

- Residual moisture in via after etch occupies a space that creates voids when W is deposited [4].
- Insufficient filling of via increases the via resistance [4].
- Via misalignment affects connecting areas and via size causing via resistance increases [4].
- Aluminum pushup at high temperatures. This occurs when Al partially fills the lower portion of the via prior to W deposition. Stress void forces (temperature coefficient expansion) tend to separate the Al/W interface upon cooling [4].
- Microcraks at the step oxide.
- Electromigration in thin metal layers.
- Other possible source of opens is the fabrication process used to decrease the poly resistance in submicron technologies (silicided opens). A layer of Ti is deposited and annealed [11] over the poly. However if the time and anneal is not correct then agglomerations inside the silicide can take place and the silicide is not correctly connected. A resistive open can be the result.

1.2 Test of ICs

The goal of the test of the integrated circuits is to identify those fabricated circuits which do not satisfy the initial specifications. The test of an IC has the following steps (See Figure 1.4):

1. Apply the input vectors to the controllable inputs of the circuits. These input vectors sensibilize the defect and propagate the possible error to an observable output.
2. A measurement is made in an observable output.
3. The measured value is compared against a reference value to determine if the circuit is accepted as fault-free or rejected.

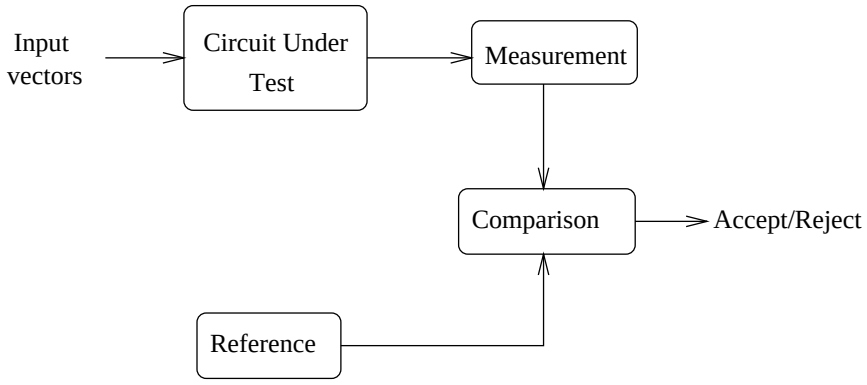
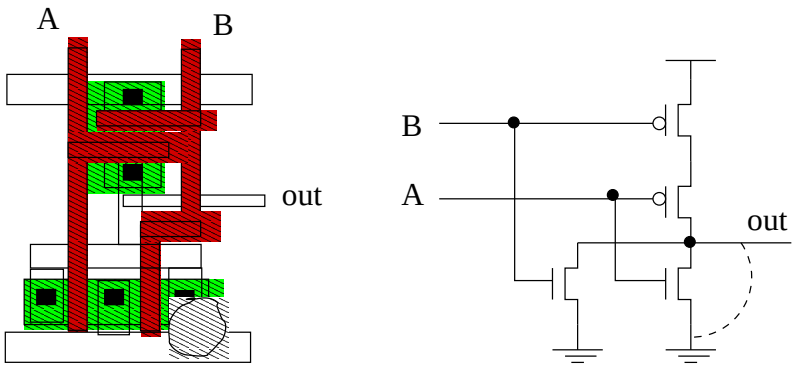


Figure 1.4: General test diagram.

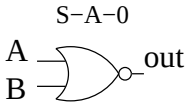
For testing the ICs the physical defects are represented adequately in a superior level of abstraction. This representation is used for test patten generation. To obtain, this fault models [12] [13] are defined which describe the effect of the physical defects in the behavior of the circuit. The fault modeling can be made at different level such as electrical, logical or functional. The most widely used fault model is the stuck-at model. In this model it is assumed that a node of a circuit behaves as always "1" or "0" logic as a consequence of the presence of a defect. Other fault models are given in the next subsection.

In Figure 1.5, it is illustrated a physical defect in a Nor gate and the representation of the defect at different abstraction levels. A physical defect as metal speck in the fabrication process connects the output node of a NOR gate to the ground line. At electrical level, the NOR gate can be represented as a resistance with a continuous range of values. The final behavior of the Nor gate depends on the sizes of the transistors of the gate and the defective resistance value of the circuit. For a low resistance values, the defect can be represented as a S-A-0 fault at logic level.

Using a defined fault model a set of vectors allowing to discriminate the response of a fault-free circuit from the faulty circuit are obtained. In this case, it is assured that the set of vectors detect those defects behaving according to the used fault model. Additionally, the set of vectors could also detect defects non behaving according to the proposed fault model. But, this detection can not be assured.



Physical Defect Electrical Representation



Logical Representation

Figure 1.5: The modeling of a fault.

1.2.1 Fault models

A good fault model should have the following properties [1] [14] :

- It should match the type of circuit in which it is to be used
- The complexity of the faults should not imply excessive computation effort
- The fault model should reflect the behavior of the physical faults with sufficient accuracy

Stuck-at fault model

One of the first proposed fault models was the **stuck-at** model. Using this fault model, Eldred [15] made a structural test for the detection of faults in the components of logic circuits. This model was further formalized and the boolean algebra used to analyze the effect of these faults in combinational circuits [16] [17]. The stuck-at model considers two possible faulty cases for every node [15]: a) a node fixed to 1 logic (stuck-at 1), and b) a node fixed to 0 logic (stuck-at 0). In the stuck-at fault model, the set of vectors is applied to the primary inputs of the circuit to sensitize the fault. The error is propagated to a primary output. Some of the characteristics of this model can be summarized as:

- Many different physical defects may be modeled by the same logic
- The complexity is greatly reduced
- The stuck-at model is technology independent
- Single stuck-at test covers a large percentage of multiple stuck-at
- Single stuck-at test covers a large percentage of unmodeled physical defects

In spite of the great advantages of the stuck-at fault model, it has been found that this model is not adequate to represent some defects in CMOS technologies [18] [19] [20] [21]. Because this other fault models have been proposed.

Stuck-open fault model

The **stuck-open** model was proposed by Wadsack [22] in the middle of 70's. This model considers that the affected transistor can remain off. The affected CMOS gate behaves as if it has memory. One test vector is not enough to detect a fault. This is illustrated with Figure 1.6.

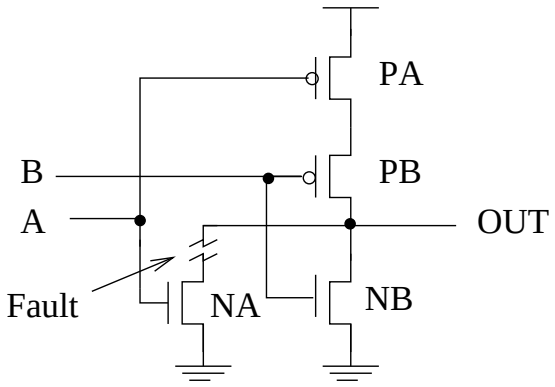


Figure 1.6: A faulty CMOS Nor gate.

Suppose that a fault takes place in the drain of NA transistor. The test vector A=1, B=0 to detect the fault may be used. The conducting path through NA transistor is not activated due to the open. Because this, the defect is not detected if the output value is at low logic level when the test vector (A=1, B=0) is applied. A two test vector strategy must be used to detect this fault. The first test vector is called initialization. This vector puts the logic value that defective transistor should change if the fault does not exist. The second test vector sensibilizes a path through the defective transistor. Logic transition at the output node is expected. If there is not transition the fault is detected.
For the case of Figure 1.6 the test vector A=0, B=0 defines a high logic value at output node (initialization). After that the test vector A=1, B=0 tries to enable NA transistor. Because the fault, transistor NA is not activated and output node does not change. Hence, the fault is detected.

Stuck-on fault model

The **stuck-on** model is used to model a defect causing a permanently transistor on. The fault model for this defect is a short. Because this, both the Pmos and the Nmos networks of a CMOS circuit may conduct [23] [24]. The fault is detectable depending upon the resistance of the defective transistor.

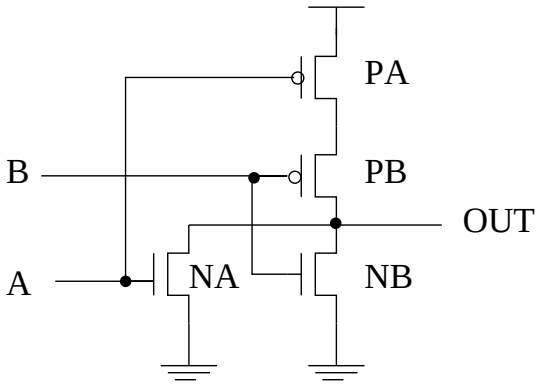


Figure 1.7: CMOS OR gate.

An example of stuck-on fault in a static CMOS two input NOR gate (See Figure 1.7) is analyzed. A stuck-on fault in NB transistor may be detected by A=0, B=0 test vector. In this faulty configuration, the output voltage V_{out} is defined according with the following equation:

$$V_{out} = \frac{R_{NB}}{R_{NB} + R_{PA} + R_{PB}} V_{DD} = \frac{R_{NB}}{R_{NB} + 2R_P} V_{DD}$$

Assuming that the drain to source resistances of both Pmos transistors are similar and a small drain to source resistance of NB transistor, the output voltage is near to logic 0. Under this condition the fault is detected. However, the fault may not be detected as R_{NB} increases.

Bridging fault model

Bridging fault model [25] [26] [27] [28] [29] is an extension of the stuck-at fault model to shorts between interconnecting lines. The model assumes that both interconnection lines will have the wired-AND or the wired-OR logic value. Bridging faults can be classified as next:

- Bridging in a logic element without feedback.- The analysis is done at transistor level. Some of the internal nodes are not characterized by logic 1 or logic 0.
- Bridging between two logic elements without feedback.- In this class only the bridging nodes are take into account.
- Bridging with feedback.- The analysis is more complex for this class because one node can depend on other node. Stability at bridging nodes is not assured. Oscillations can result.

In [30] controllability conditions to observe bridging defects are shown for combinational and sequential circuits. Physical factors such as transistor ratio size and bridge resistance determine the controllability conditions. Also the diagnosis of bridging can also be realized without physical information [31]. The possibility of occurrence of a bridging is determined by two techniques. The first one identifies a bridged node and the second one identifies the candidates according with the expected faulty behavior.

1.2.2 Logic testing

Logic testing [14] is used to monitor the logic levels (Boolean values) of circuits under test (CUT). Every circuit have a characteristic logic function. The output node of a CUT shows a defined logic value for a given combination of the inputs. Logic testing compares the response of the output node of the CUT versus the expected fault-free response of the CUT. If both results are not the same the CUT is faulty. In logic testing, it is assumed that a sufficient time is waited after the vector application at the input for the output to settle to stable levels.

1.2.3 I_{DDQ} testing

Current testing is used to monitor the current of the power supply of the CUT instead of monitoring the logic levels. Some defects can produce intermediate voltages and the methods based in logic levels are not efficient. This method uses the property of the CMOS circuits that in steady state there is not flow current through the circuit. The leakage current is assumed negligible.
Suppose a CMOS NAND gate (See Figure 1.8) with a stuck-on in the source-drain terminals of transistor NB. The input applied vector A=1, B=0 should charge to node OUT, however because the bridge, the Nmos network is active and a current path from V_{DD} to ground is created. NAND gate is detected as faulty because a high quiescent current consumption (I_{DDQ}) appears.

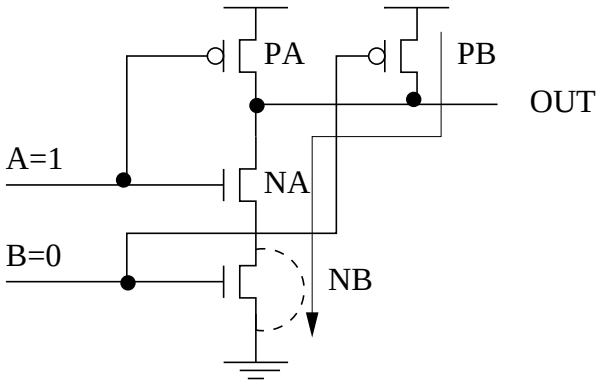


Figure 1.8: A faulty CMOS NAND gate.

I_{DDQ} current test demonstrated to be adequate to detect defects as bridging [26] and certain open defects [32]. However, as the technology scales the detection of some defects is missing. Not only simple current measurements have been used but also more elaborate strategies as current signatures [33] [34]. The information of defective circuits is contained in the level and the magnitude of the static current. High leakage current due to defects could be detected by the current signature. The detectability of I_{DDQ} has been increased by the concept of variable current thresholds [35]. Also layout-based test generation have been proposed [36]. Using layout, a fault list is created taking into account realistic defect representations. The methodology is oriented to current testing but it can

also be used to voltage oriented testing.
Differential I_{DDQ} has also been proposed [37]. Differential I_{DDQ} is limited by leakage currents. The proposal of Kruseman [37] is not efficient for off-state currents above 100mA. Cooling techniques [38] can be used to counter at the effect of subthreshold currents. Sachdev [39] has proposed other solutions to this I_{DDQ} limitation.

1.2.4 Delay testing

Delay testing is not based to assure the logic levels of the CUT. Instead of that, the timing conditions of the observed nodes are assured to be under design specifications. The delay model can be principally divided into gate delay model and path delay model [40]. The gate delay model [41] is based in testing the timing specifications of the selected device. However, cumulative delay variations from previous gates escape to this model. Path delay model resolves this problem [42]. A path is selected to be the target for measure the delay, then $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions are propagated through the path. If the measured delays are inside of the observation window then the path is fault-free, otherwise the path is faulty. The observation window can be defined close to the functional timing of the path in statistical distributions of delay [43].
In [44] [45] it is demonstrated that the measured delay not only depends on delay gate but also on the gates that are before and after that target gate, where two or three vectors are employeed to obtain the maximum delay. Delay testing showed to be an adequate testing tool in order to detect fault mechanisms as resistive opens and resistive bridges for sub-micron technologies [46].

1.3 Complexity of testing of opens

Because the scaling of the technology some trends will affect the actual testing methodologies [47] [48]. Some faults may escape to conventional test methods. Non-conventional test methods [49] [50] should be used. According with [47] [51] the test strategies should move to structural testing. This would allow to obtain

a higher quality, lower delivering time to the market, among others.

A significant research effort has been devoted to test of opens [52] [53] [54] [32] [55] [56] [50] [57]. It has been found that breaks is an important contributor to test escapes [58] [49]. The problem has became worst with scaling of the technologies. The trends have increased sensitivity to subtle defects [49]. Subtle defects increases the delay for a small amount but they didn't cause a functional failure. However, for circuits running at higher speeds a system failure can occur. It has been found that full opens have a complex behavior [52] [53] [57] [32]. The detectability of this defect depends on technology and topology parameters. Furthermore, its behavior also depends on the gate oxide trapped charge [59] [55]. Needham et al. [58] have found that test of opens would require special temperature, voltage and timing conditions. Silicided open defects need to be tested at low temperature [11]. Delay fault testing has been suggested to be used to test resistive vias/contacts [4]. From simulation data it has been found that resistive opens have a significant range of resistances increasing the delay [60]. A high resistance value is required for a stuck-at to occur. This makes a stuck-at based test less effective for opens. In addition, opens are more difficult to sensitize [61] [60]. Other authors [46] have pointed-out that crosstalk [62] [63] and power rail coupling [46] influences the detectability of resistive opens.

1.4 Organization of the thesis

This thesis is organized as follows: in Chapter II, the detectability of full opens in interconnections by logic and I_{DDQ} testing is investigated. Testability regions are determined using simple analytical expressions. The layout topology of the circuit have been taken into account. In Chapter III, the behavior and detectability of resistive opens in CMOS memory elements are investigated. The analysis is extended to a scan path chain. In Chapter IV, an X-Y zoning method is proposed to explore verification of time critical digital signals. Finally, in Chapter V, the conclusions of the thesis are given.

Chapter 2

Full Opens.

2.1 Introduction

In this chapter, the behavior full of interconnection opens is investigated. Conditions to test interconnection opens by logic and I_{DDQ} testing are determined. Opens in interconnection paths disconnect the driven gate(s) from the driving gate. Due to the break the Pmos and Nmos transistor connected gates of the driven gate(s) float.

From experiments made on ISCAS'85 benchmark circuits, it has been found that interconnection opens have the highest probability of occurrence among the different types of opens [64]. Vias are a likely place for an open to occur [4] [2] [65] [3] and there are a high number of vias in actual process due to the many metal levels [65] [3]. Breaks defects have been found to be an important contributor of test escapes [58]. The behavior of floating connected gates due to an interconnection open has been investigated since the late eighties [54] [53] [59] [52] [66] [67]. It has been found that some circuits with these defects work logically correctly at low frequencies, but fail at higher frequencies [53] [66]. Other researches have observed a stuck-at behavior and negligible quiescent current values for an inverter with a given double floating gate defect [52]. The parasitic capacitances related to the floating node determine the behavior of the defective gate [53] [68] [56] [52] [66]. In addition, tunneling effects have been found across the break for small opens [53] [69]. Singh et al. [67] have found significant values of quiescent

current on fabricated circuits intentionally designed with double floating gate defects. The defects were also detected by output logic monitoring. The trapped charge on the floating gate during fabrication process may influence significantly the behavior of interconnection opens [59] [55] [70]. In addition, the voltage at the floating wire can also be influenced by the die surface effect observed by Konuk and Ferguson [55]. More recently, it has been found that floating gates due to interconnection open may present oscillations and sequential behavior [56]. Konuk [68] [71] have analyzed the testability of interconnection opens under a voltage (stuck-at) and current based test. A fault simulator for interconnect opens which take into account almost all the factors that can affect the voltage at the floating line has been developed [66] [55]. Renovell et al. proposed a electrical model using the twin-transistor structure in order to cope unpredectible parameters as initial charge and polysilicon to bulk capacitance [70]. Champac et al. have studied the detectability of interconnection opens by logic and I_{DDQ} testing [72].

In this work, the detectability of full interconnection opens by logic and I_{DDQ} testing is investigated. A coupling capacitive model which takes into account technology and topology parameters has been developed. Using this model, explicit compact analytical expressions are obtained to determine the conditions for reliable detection of these opens by logic and I_{DDQ} testing. Testability regions in order to guarantee logic and I_{DDQ} testing are obtained from the analytical expressions. Reliable testing conditions of the open is considered in this work. Well defined logic "0" and "1" levels at the input of a gate have been considered as V_{TN} and $V_{DD} - |V_{TP}|$, respectively. In this work, it is also investigated the influence of the circuit topology in the detectability of the open. As a consequence of the circuit topology the optimum test vector to excite the open may not be generated. Three possible situations are analyzed: full controllability, partial controllability and low controllability. The effect of the initial trapped charge is also considered. Line spacing is used as a routing design technique in order to make detectable those opens non detectable by either stuck-at testing or I_{DDQ} testing. Finally, the influence of unsensitized gates is analyzed.

The rest of this chapter has been organized as follows: in Section 2.2, the

modeling of interconnection opens is presented. In Section 2.3, logic and I_{DDQ} testability of interconnection opens is analyzed. In Section 2.4, the detectability conditions for interconnection opens using the proposed coupling model are investigated. In Section 2.5, routing design for testability techniques for non detectable interconnection opens are explored. In Section 2.6, the influence of unsensitized gates is analyzed. Experimental measurements are presented in Section 2.7. Finally, in Section 2.8 the conclusions of the chapter are given.

2.2 Modeling of interconnection opens

Opens in interconnections produce NMOS and PMOS connected gates of the affected gate to float. In Figure 2.1, a typical defective topology of a circuit in the presence of an interconnection open is shown. Large breaks are assumed so there is a non-significative influence (e.g. tunneling effect [53] [69]) from the input signal (See Figure 2.1) on the floating line.

In this case, the behavior of a gate(s) with an interconnection open is determined by the voltage at the floating node (V_{if}). This voltage depends on the transistor structure of the affected gate(s) modeled by its gate charge [32] [73] [74], the surrounding capacitances to the floating line [32] [53] [52] [66] and the trapped charge during the fabrication process [59] [55]. An electrical model for an interconnection open is shown in Figure 2.2 where five topologies are identified:

- **The Nmos topology** is formed by the gate-source Nmos overlap capacitance (C_{gson}), the poly-bulk capacitance (C_{pb}) of the floating line and the influence of the intrinsic part of the Nmos transistor.

- **The Pmos topology** is formed by the gate-source Pmos overlap capacitance (C_{gsop}), the poly-well capacitance (C_{pw}) of the floating line and the influence of the intrinsic part of the Pmos transistor.

- **The feedback topology** that takes into account the gate-drain Pmos overlap capacitance (C_{gdop}) and the gate-drain NMOS overlap capacitance (C_{gdon}).

- **The coupling topology** that takes into account the effect of the coupling capacitance from neighbors lines, lower and upper metal layers.

- **The routing topology** that takes into account the running metal layer capacitance. One part of this capacitance runs over the well and the other one over the substrate.

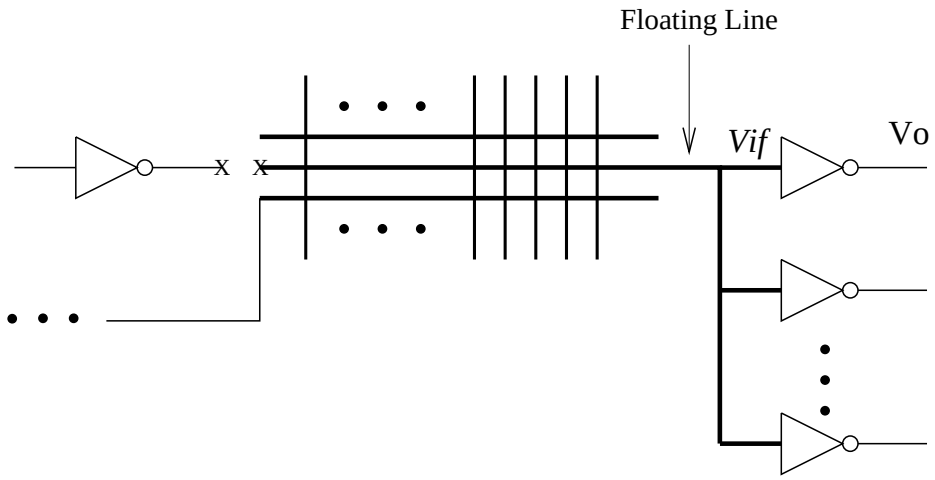


Figure 2.1: A typical defective circuit topology.

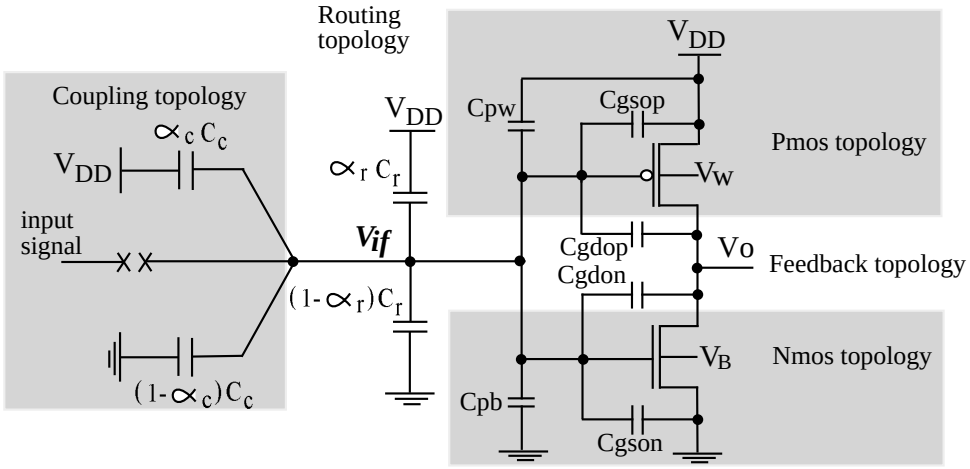


Figure 2.2: Electrical model for an inverter with an interconnection open at its input.

According to the law of charge conservation at the floating node, the following equation must be satisfied:

$$\begin{aligned} Q_{tr} &= NQ_{GTN} + NQ_{GTP} + NQ_{Cgson} + NQ_{Cgdon} + NQ_{Cgsop} + NQ_{Cgdop} + Q_{Cpw} \\ &\quad + Q_{Cpb} + Q_{Cr} + Q_{Cc} \end{aligned} \tag{2.1}$$

where Q_{tr} is the trapped charge at the gate oxide during fabrication, Q_{GTN} and Q_{GTP} are the induced charges at the floating gates by the intrinsic part of the transistors, Q_{Cgson}, Q_{Cgdon}, Q_{Cgsop}, Q_{Cgdop} are the charges induced by the overlap capacitances, Q_{Cpw}, Q_{Cpb} are the induced charges at the floating node by the poly-well and poly-bulk capacitances, Q_{Cr} and Q_{Cc} are the related charges to the break position, Q_{GTN} and Q_{GTP} are given by functions of the terminal transistors voltages [75].

Relating the charges to the capacitances and the voltage across them, and after rearranging, an expression for the voltage at the floating node V_{if} is obtained.

$$V_{if} = \frac{NC_{gsop} + C_{pw}}{C_T} V_{DD} + \frac{N(C_{gdon} + C_{gdop})}{C_T} V_o - \frac{NQ_{GT}}{C_T} + V_{DD}\frac{\alpha_c C_c}{C_T} + V_{DD}\frac{\alpha_r C_r}{C_T} + \frac{Q_{tr}}{C_T} \tag{2.2}$$

where $C_T = N(C_{gson} + C_{gdon} + C_{gsop} + C_{gdop}) + C_{pb} + C_{pw} + C_r + C_c$

$Q_{GT} = Q_{GTN} + Q_{GTP}$

$\alpha_c = \frac{C_c^{V_{DD}}}{C_c}$

$\alpha_r = \frac{C_r^{V_{DD}}}{C_r}$

The floating line can be influenced by signals running at adjacent coupling lines and/or by lines located above/below the floating line (See Figure 2.1). The location of the break influences the values of the two defect topology parameters:

a) The floating routing capacitance C_r.- Part of C_r may have one terminal connected to the bulk which is biased to V_{GND} (in the technology we used) and the other part to the well which is biased to V_{DD} (See Figure 2.2). This is modeled by α_r representing the fraction of floating routing capacitance with one terminal connected to the well. In this work, it has been assumed that the floating routing track runs over the bulk (bulk is at ground potential). This takes into account a typical situation where most of the routing runs over the bulk (V_{GND}). However, the results can also be extended for those cases with part of the floating routing running over the well (V_{DD}).

b) The coupling capacitance to the floating line C_c.- The signals at the adjacent lines to the floating one influence significantly the voltage at the floating line. The signals at the adjacent lines may have a high logic value (V_{DD}) or a low logic value (V_{GND}). α_c represents the fraction of the coupling capacitance with a high logic value (V_{DD}).

Equal-sized inverters are assumed. But, the model can be extended to consider different-sized inverters and other sensitized gate structures. The effect of non-sensitized gate inputs [68] is considered in subsection 2.6.

Conditions for feedback wire-to-wire and Miller capacitances producing oscillating and sequential behaviors [56] are not considered in the proposed model.

The behavior of a gate with an interconnection open also depends on the trapped charge deposited during fabrication Q_{tr} [59] [55]. As mentioned above experiments by Konuk and Ferguson [55] showed that the trapped charge on floating metal wires connected to transistor gates can create voltages in the range between -0.5 and 0.5V for experimental chips fabricated with an HP 0.8μm process.

2.3 Logic and I_{DDQ} Testability

In this section the logic and I_{DDQ} testability of interconnection opens are investigated. It has been considered that one inverter has its gate floating due to the defect. The inverters are minimum symmetrically-sized gates. In addition, it has been considered that the lines can be laid-out in the first metal layer (e.g metal 1) or in the upper metal level (e.g metal 4). The logic and I_{DDQ} testability of interconnection opens have been investigated through the parameters L_r, L_c. L_r models the length of routing from the floating connected gates to the break location. L_c models the length of routing adjacent to the floating line. Minimum distance allowed by the design rules are used for the two lines L_r, L_c. As an N-well technology is used, it has been assumed that the total floating routing capacitance has one terminal connected to the bulk.
The difference between logic and I_{DDQ} testing is given by the transfer inverter function (See Figure 2.3). The voltage at the floating gate (See Figure 2.2) defines the testability of the inverter:

I) When the input voltage is lower than Nmos threshold voltage, the current through device is almost zero. This condition is assured logic testable and non I_{DDQ} testable.

II) When the input voltage is greater than $V_{DD}-|V_{TP}|$, the current through device is almost zero. This condition is assured logic testable and non I_{DDQ} testable.

III) When the input voltage has a value between V_{TN} and $V_{DD}-|V_{TP}|$, so the device is in the high gain region, a quiescent current path from V_{DD} and ground exists. This condition is non assured logic testable and assured I_{DDQ} testable.

Logic Testability

The voltage at the gate depends on the defect topology parameters (L_r and L_c). It has been found that intermediate voltages for both type of signals at the adjacent line appear for short lengths of the adjacent line (See Figure 2.4). Hence, logic testability can not be assured for these defects. As the value of L_c increases the output voltage goes to well defined logic levels. The influence of

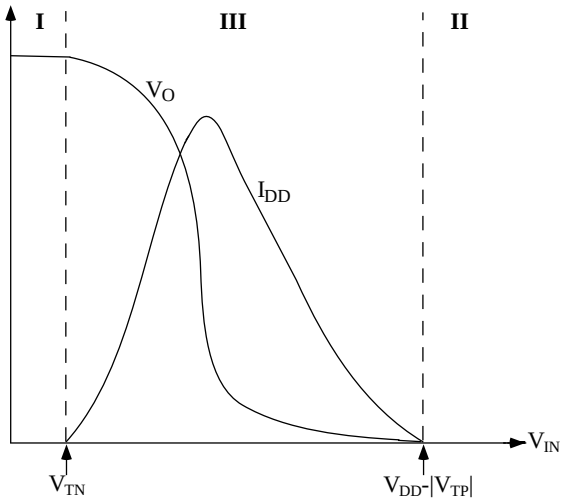


Figure 2.3: Quiescent current regions.

L_c over the floating node is smaller for interconnection opens located in lower metal levels (See Figure 2.4) than for those located in upper metal layers (See Figure 2.5). This is because for upper metal layers the capacitance of the line to ground per unit length decreases significantly with respect to the lower metal layers. As a consequence the influence of the coupling layers increases. Because this, intermediate voltages appear for lower values of L_c.

I_{DDQ} Testability

A current path between power supply and ground is established when the input gate voltage reaches the range between V_{TN} to $V_{DD} - |V_{TP}|$. This range voltage can not be logically assured instead of that I_{DDQ} is used. Interconnection opens are I_{DDQ} detectable for short lengths of the adjacent coupling line (See Figure 2.6 and 2.7). For lower metal layers, significative I_{DDQ} values are obtained when 1→0 adjacent line transitions and small routing length are employed (See Figure 2.6). For upper metal layers and not very large coupling length give significative I_{DDQ} values. However 1→0 transitions, the routing and coupling length are wider for upper metal layers than for lower metal layers.

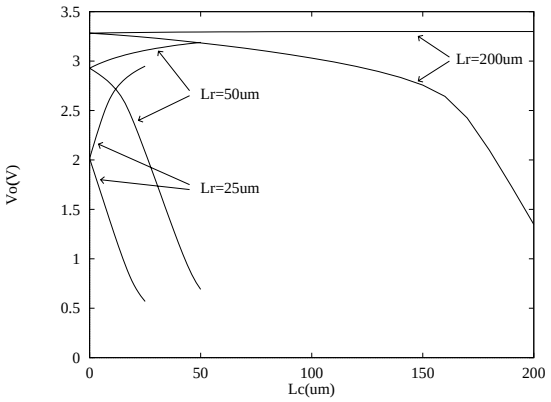


Figure 2.4: Output voltage characterization for an inverter with an interconnection open at its input. Curves going up: 0V at the adjacent coupling line. Curves going down: V_{DD} at the adjacent coupling line. Signals running in metal 1 layer.

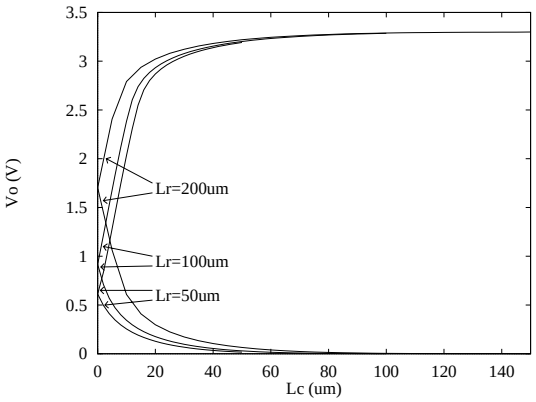


Figure 2.5: Output voltage characterization for an inverter with an interconnection open at its input. Curves going up: 0V at the adjacent coupling line. Curves going down: V_{DD} at the adjacent coupling line. Signals running in metal 4 layer.

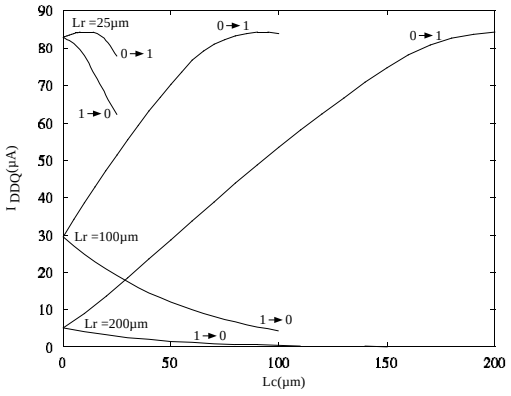


Figure 2.6: I_{DDQ} characterization for an inverter with an open interconnection at its input. Signals running in metal 1 layer.

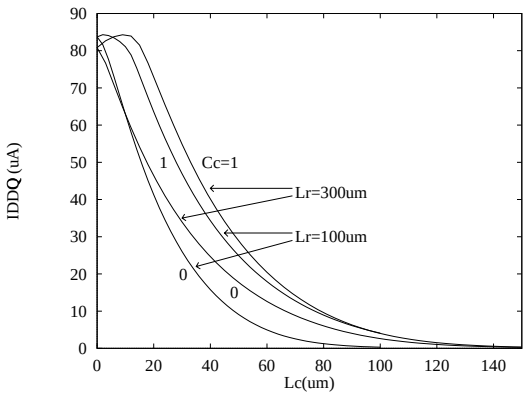


Figure 2.7: I_{DDQ} characterization for an inverter with an open interconnection at its input. Signals running in metal 4 layer.

2.4 Detectability Conditions for Interconnection Opens

In this section, the detectability conditions to test full opens in interconnection are investigated. The dependency of the detectability of this defect on the signal at the driving gate and coupling lines is investigated. A circuit similar to that shown in Figure 2.1 has been considered. Two inverters of minimum symmetrical-sized inverters float due to the open. It has been assumed that the initial trapped charge is negligible (i.e. Q_{tr}=0). The effect of non-zero initial trapped charge has been analyzed in [72]. It has been assumed that the floating routing track runs over the bulk. This means that α_r is equal to zero in equation 2.2. It is also assumed that there is no initial trapped charge.

The floating node can be influenced for different coupling lines (See Figure 2.1). A schematic representation is shown in Figure 2.8. All the possible exciting vectors, assuming that all the coupling lines can be simultaneously controlled to 1 or 0 logic, are shown in Table 2.1. The detectable ranges are also given. For an I_{DDQ} based testing the fault only must be sensitized. Propagation of the fault is not required. However, for a stuck-at based testing the fault must be sensitized and the faulty behavior must be propagated to a primary output. Consequently, the vector generation process is more complex for a stuck-at based testing than for I_{DDQ} testing. We will assume that the test vector generation for I_{DDQ} testing can sensitize properly the defective gate. However, the possible exciting vectors for a stuck-at based testing depends strongly on the topology of the circuit. The testability regions of four possible situations are analyzed:

- Full controllability
- Partial controllability
- Low controllability
- Initial trapped charge

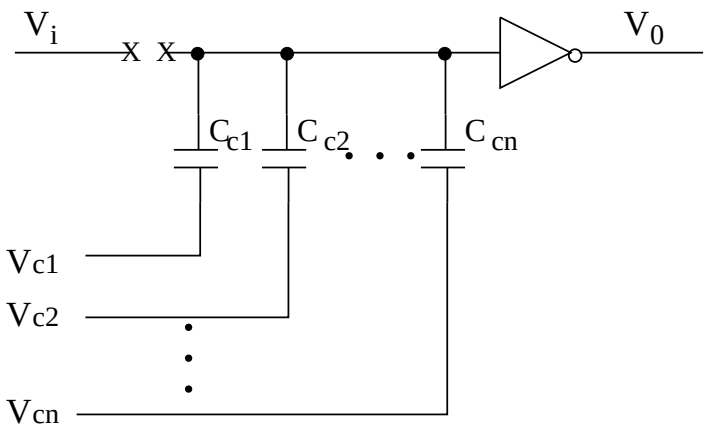


Figure 2.8: Circuit to illustrate the possible test vector conditions for an interconnection open.

2.4.1 Full controllability case

For this case, all the test exciting vectors of Table 2.1 can be generated. High logic levels at V_{ci} signals (See Figure 2.8) help to detect stuck-at 1 faults at the floating node. Low logic levels at V_{ci} help for a fault-free behavior of the defect. Hence the open may not be detected. The opposite is true for a stuck-at 0 fault at the open. The two most favorable exciting vectors for a stuck-at based testing of the interconnection open can be generated for the full controllability case. For a vector detecting a stuck-at-0 (stuck-at-1) fault at the open, all the coupling lines are at V_{GND} (V_{DD}). For the simple inverter case. I_{DDQ} detectability is considered just depending on the value of the coupling signal. However, for other gates the required vector for I_{DDQ} testing must create a sensitized path between the power supply and ground through the defective floating Pmos and Nmos transistors.

V_i	$V_{ci}...V_{cn}$	Detectable range V_{if}	Fault
0	0	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
0	1	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
1	0	$[0, V_{TN}]$	SA-0
1	1	$[0, V_{TN}]$	SA-0

Table 2.1: Possible test vector condition.

The logic threshold is normally used as a reference to determine faulty/fault-free behavior. However, in deep submicron technologies parameter variation and noise may invalidate the gate threshold reference [76]. Those defect topology parameters C_r, C_c producing voltages at the floating node between V_{TN} and $V_{DD} - |V_{TP}|$ have ben considered I_{DDQ} testable and non-assured logic testable. Using the proper input vector, those defect topology parameters producing voltages at the floating node lower than V_{TN} or greater than $V_{DD} - |V_{TP}|$ have been considered non-I_{DDQ} testable and assured logically testable.
Considering the value of the signal at the adjacent coupling line and the assured testable voltages at the floating node, the following conditions are found:

- Guaranteed V_{TN} with C_c at V_{DD}
- Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{DD}
- Guaranteed V_{TN} with C_c at V_{GND}
- Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{GND}

Guaranteed V_{TN} with C_c at V_{DD}

The necessary conditions to assure an induced voltage at the floating node no greater than the threshold voltage of the n-channel transistor will be obtained. Taking into account the static transfer curve of an inverter [77], the output voltage will have a value very close to V_{DD} at V_{if}=V_{TN}. At this point, the p-channel transistor operates at the linear region and the n-channel transistor is in the boundary between saturation and cut-off [77]. We assume that the n-channel transistor operates in the cut-off region.

Relating the charges to the capacitances and the voltage across them, after substituting V_{if}=V_{TN} and V_O=V_{DD} in equation 2.2, an explicit expression can be obtained to estimate the minimum floating routing capacitance (C_r^*) to have at most an induced voltage of V_{TN} for a given value of the coupling line capacitance (C_C). This gives the following equation:

$$C_r^* \geq \frac{C_{DD}(V_{DD} - V_{TN}) - (NC_{gson} + C_{pb})V_{TN} - NQ_{GT}}{V_{TN}} \tag{2.3}$$

where C_{DD}=$N(C_{gdon} + C_{gdop} + C_{gsop}) + C_{pw} + C_C$

Q_{GT}=$Q_{GTN} + Q_{GTP}$

Q_{GTN}=$C_{oxn}\gamma_N \left(-\frac{\gamma_N}{2} + \sqrt{\frac{\gamma_N^2}{4} + V_{TN} - V_{FBN}} \right)$

Q_{GTP}=$C_{oxp}[(V_{TN} - V_{DD} + |V_{TP}|) - \gamma_P\sqrt{-2\Phi_{FP}}]$

where C_{oxn} and C_{oxp} are the gate oxide capacitance of the Nmos and Pmos transistors, γ_N and γ_P are the body factors of the Nmos and Pmos transistors, V_{FNB} is the flatband voltage of the Nmos transistor, Φ_{FP} is the Fermi potential of the Nwell.

Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{DD}

In this case conditions to assure a voltage no lower than $V_{DD} - |V_{TP}|$ at the floating node are obtained. In this way it is assured a low voltage at the output inverter. Under these voltages conditions the Nmos transistor operates in the linear region and the Pmos transistor operates in the border between saturation and cut-off, the last region can be assumed. After substituting all these conditions in equation 2.2, an expression is obtained which determine the maximum floating routing capacitance (C_r^*) allowed to have at least an induced voltage of $V_{DD} - |V_{TP}|$ at the floating node.

$$C_r^* \leq \frac{C_{GG}(V_{DD} - |V_{TP}|) - (NC_{gsop} + C_{pw})(|V_{TP}|) - NQ_{GT}}{V_{DD} - |V_{TP}|} \tag{2.4}$$

where C_{GG}=$N(C_{gson} + C_{gdon} + C_{gdop}) + C_{pb} + C_r$

Guaranteed V_{TN} with C_c at V_{GND}

The expression to estimate the minimum routing capacitance (C_r^*) to have at most an induced voltage of V_{TN} is:

$$C_r^* \geq \frac{C_{DD}(V_{DD} - V_{TN}) - (NC_{gson} + C_{pb})V_{TN} - NQ_{GT} - C_c(V_{DD})}{V_{TN}} \tag{2.5}$$

Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{GND}

The expression to estimate the maximum floating routing capacitance allowed to have at least an induced voltage of $V_{DD} - |V_{TP}|$ at the floating node is:

$$C_r^* \leq \frac{-C_{GG}(V_{DD} - |V_{TP}|) - (NC_{gsop} + C_{pw})(|V_{TP}|) - NQ_{GT}}{V_{DD} - |V_{TP}|} \tag{2.6}$$

Using the previously developed expressions, the testability regions on the C_r-C_c plane can be identified for interconnection opens (See Figure 2.9).

1. I_{DDQ} + Logic Testing.- Two separate regions appear:
   - A significant range of the defect topology parameters are both I_{DDQ} and logic testable (See Figure 2.9). These defects are assured logically testable for a vector detecting a stuck-at-0 fault (coupling signal is low) at the open.
   - A small range of the defect topology parameters are both logically (stuck-at-1 vector) and I_{DDQ} (coupling high) testable.
2. Only Logic Testing.- A range of the defect topology parameters are only logically testable. A stuck-at-0 vector is required for large lengths of break locations (large C_r) and small coupling values. Either a stuck-at-0 or a stuck-at-1 vector detects interconnection opens for large coupling values and small floating routing capacitance. The latter case is more likely to

appear when most of the floating routing and coupling occurs in upper metal layers. This is because the capacitance of the line to ground per unit length is lower for upper metal layers than for lower metal layers.

3. Only I_{DDQ}.- Intermediate voltages appear for a significant range of the defect topology parameters for both types of signals at the coupling line (See Figure 2.9). Hence, logic testability can not be assured for these defects. These defects can be detected by I_{DDQ} testing no matter the value of the coupling signal. This region is more significant for opens located in upper metal layers than for those in lower metal layers.

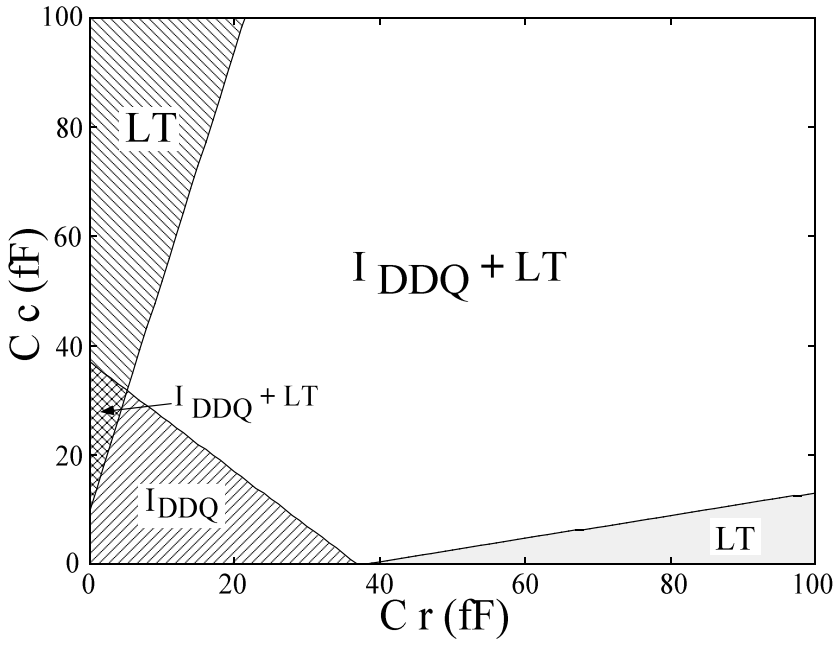


Figure 2.9: Testability regions for interconnection opens. Full controllability case. LT: assured logic testability.

The previous analysis suggest that the stuck-at based testing will have a higher likelihood to detect the open for stuck-at 0 (stuck-at 1) fault when:

- Most of the coupling signal(s) are controlled low (high) when most of the floating routing runs over the bulk (well). The well is connected to V_{DD} in the technology that we used.

I_{DDQ} testing tends to be more efficient to detect the open when:

- The influence of the floating routing and coupling capacitances are opposite. Most of the coupling signal(s) are controlled high (low) when most of the floating routing runs over the bulk (well).

2.4.2 Partial controllability case

In this case, the coupling signals can not be controlled simultaneously at 1 or 0 logic. Hence some of the most favorable conditions (See Table 2.1) to test the interconnection opens can not be generated. A simple circuit illustrating a situation where controllability for certain conditions can not be generated is shown in Figure 2.10.

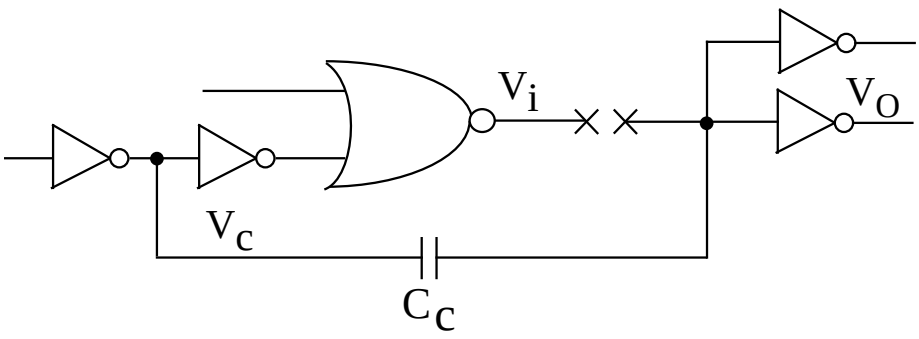


Figure 2.10: Schematic circuit where one of the most favorable condition for a stuck-at testing can not generated.

For this circuit, the vectors V_i V_c= 00, 01, 11 can be generated. However, the vector V_i V_c=10 can not be generated. It must be noted that this vector is the most favorable condition for a stuck-at 0 fault at the open.

Konuk et al. [56] have suggested that a large amount of signal wires running perpendicularly to the floating wire tend to bias the floating wire to $V_{DD}/2$. This is because about half of coupling signals have a high probability to be a logic 1 and the other half at logic 0. For the coupling of adjacent wires to the floating

wire this probability may decrease for a small number of adjacent wires. The effect of partial controllability of the coupling signals has been considered for the case where one half of the coupling capacitance is at 1 (V_{DD}) and the other is at logic 0 (V_{GND}). The previous developed expressions have been modified to consider this condition. Using the modified expressions, the testability regions have been determined (See Figure 2.11):

- Only I_{DDQ}.- A significant range of the defect topology parameters is testable only by I_{DDQ} testing.

- Only Logic Testing.- A range of the defect topology parameters is guaranteed logically testable. A stuck-at-0 vector is required. The range of defect topology parameters detectable by a stuck-at based testing is significantly smaller than for full coupling controllability. This range does not even appear (or very small) for interconnection opens in upper metal layers.

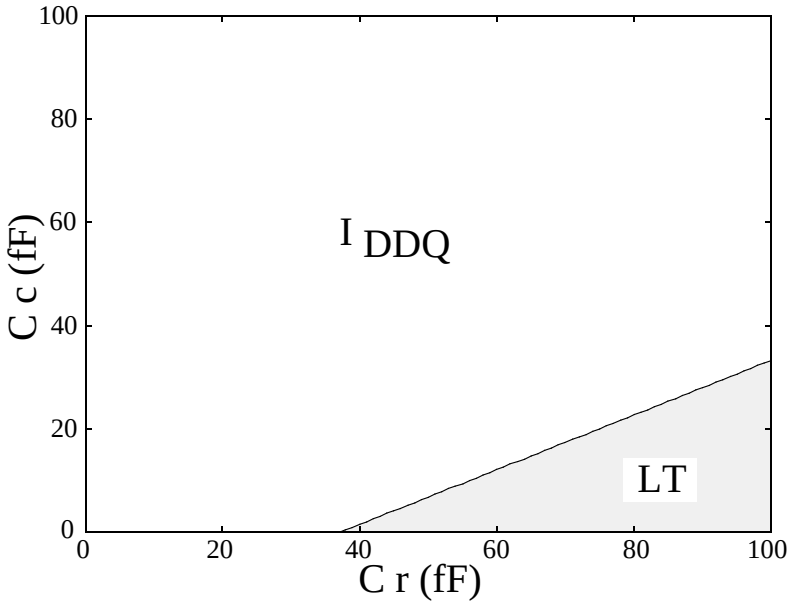


Figure 2.11: Testability regions for the partial controllability case.

2.4.3 Low controllability case

In this subsection, it is analyzed the case when the two most favorable conditions for a stuck-at based testing of Table 2.1 can not be generated. A simple circuit example is given in Figure 2.12. A simple case is when the via (contact) connecting two cascaded gates is missing (See Figure 2.13).

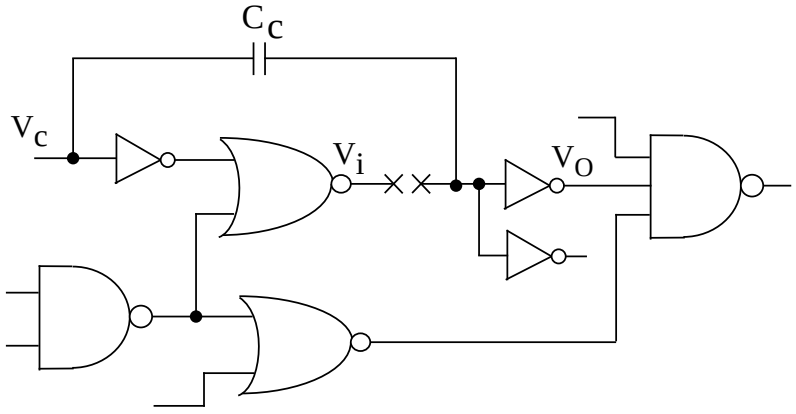


Figure 2.12: Schematic circuit where the two most favorable conditions for a stuck-at based testing can not be generated.

For the circuit shown in Figure 2.12, the vectors V_i V_c= 00, 11 can be generated. However, the most favorable stuck-at vectors V_i V_c= 01, 10 can not be generated. This can be extended to **n** coupling signals. The testability regions for this open are shown in Figure 2.14. It has also been assumed that the floating routing track runs over the bulk and there is no initial trapped charge. In this case, a large range of defects which were logic detectable for the full-controllability case are now non detectable (See Figures 2.9 and 2.14). Furthermore, a region of defect parameters (C_r, C_c) are non detectable by either a stuck-at based testing or I_{DDQ} testing (See Figure 2.14). This region is more likely to appear for interconnection opens located in upper metal layers (C_c larger than C_r). A Hspice simulation for an interconnection open non detectable by either stuck-at based testing or I_{DDQ} testing is shown in Figure 2.15. A realistic case with C_r=6fF and C_c=40fF has been considered. Routing design for testability techniques may be used in order to make detectable this type of opens.

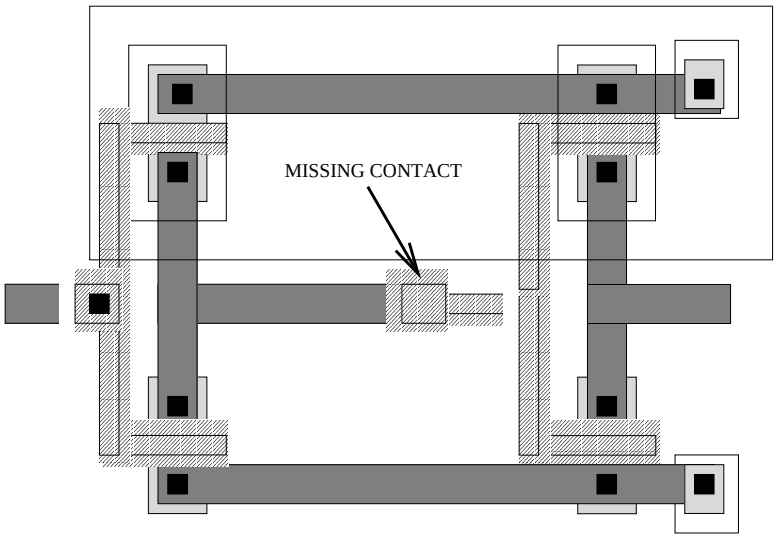


Figure 2.13: Layout of two cascaded inverters.

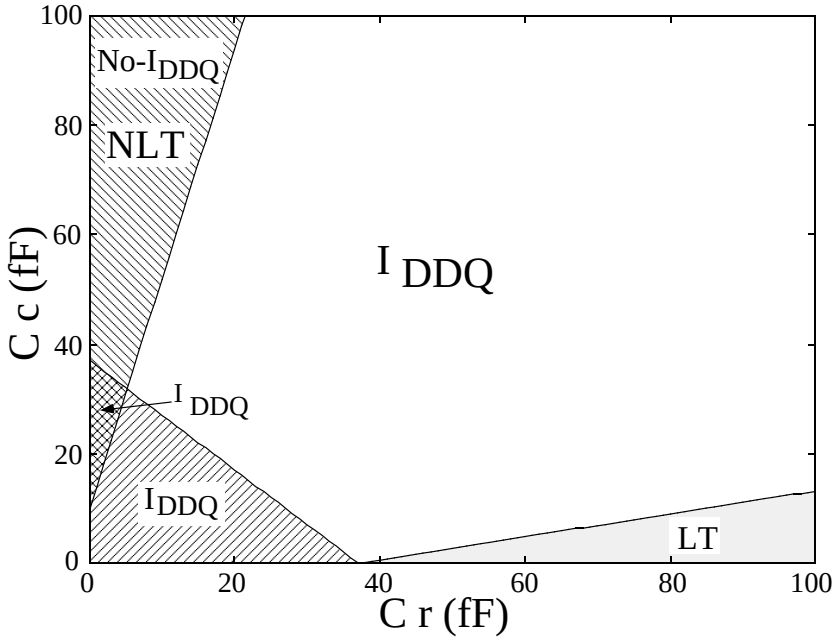


Figure 2.14: Testability regions of interconnection opens for the low controllability case.

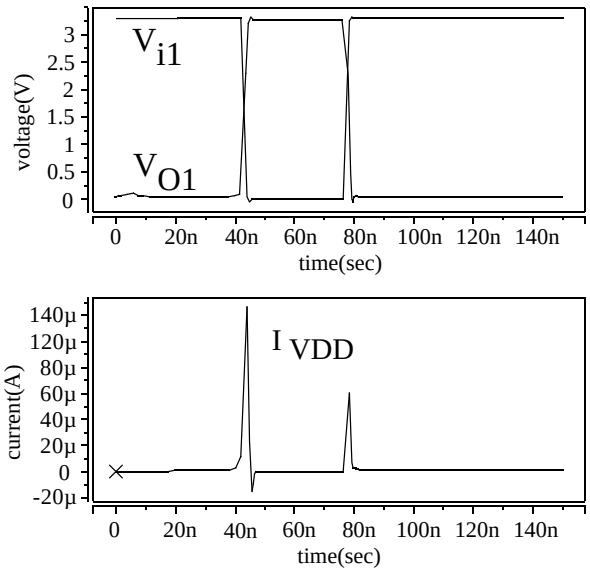


Figure 2.15: Timing diagram showing an interconnection open non detectable by either a stuck-at testing or I_{DDQ} testing.

2.4.4 Initial trapped charge

In this subsection, the influence of the initial trapped charge [59] [55] on the detectability of interconnection opens is analyzed. Full controllability for the coupling signals has been assumed, and with the total floating line running over the bulk.

The value of the trapped charge depends strongly on the technology used and on the topological considerations [59] [55] [68]. A variation of [-0.3V, +0.3V] for the initial trapped voltage has been considered. The actual values of the trapped charges are calculated considering the circuit unpowered. Rearranging equation 2.2, an expression to calculate the trapped charge is obtained.

$$Q_{tr} = NQ_{GT} + V_{tr}C_T \tag{2.7}$$

where Q_{GT} is obtained from the corresponding transistor charge equations [75] according to the operating transistor regions for the unpowered circuit, and C_T has been defined in equation 2.2.

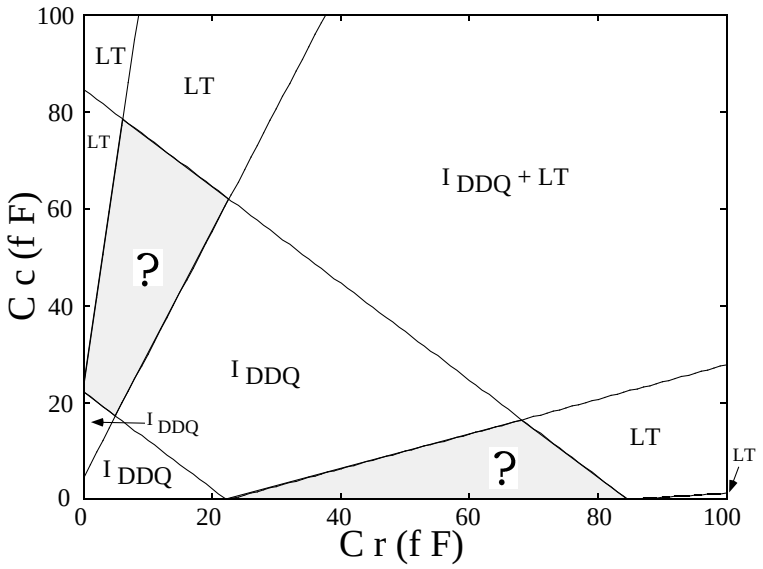


Figure 2.16: Testability regions for interconnection opens, dependency on the trapped voltage, Variation of initial trapped voltage:[-0.3V, +0.3V], LT: assured logic testability, ?: non assured either logic or I_{DDQ} testability.

The range of defect topology parameters assured logically and I_{DDQ} testable decreases due to the spread of the initial trapped voltage (See Figure 2.16). For a significant range of defect topology parameters it can not be assured which technique detects a defect in this region (See Figure 2.16). But at least one of the test techniques (logic or I_{DDQ}) will detect the defect. This range decreases (increases) as the variation of the trapped charge decreases (increases).

2.5 Routing design for testability

In this section, it is explored to use routing design for testability in order to make detectable those interconnection opens non detectable by either a stuck-at testing or I_{DDQ} testing. This analysis has been carried out through the parameter L_r and L_c instead of C_r and C_c. It has been considered one adjacent line to the floating one. The used technique separates physically the two involved adjacent lines [78]. The lines are separated until the open became either assured logic testable or I_{DDQ} testable. To accomplish this, the testability regions for the low controllability case have been obtained for a line spacing wider (5 lambdas) than

the minimum (3 lambdas) allowed by the technology (See Figures 2.17 and 2.18). In Figure 2.17, the testability regions for the case of low controllability under minimum line spacing are shown. It has been found that some interconnection opens which were non detectable by either a stuck-at based or I_{DDQ} testing under minimum line spacing (See Figure 2.17) are now detectable by I_{DDQ} testing (See Figure 2.18). Further increases of the line spacing, it will make detectable other interconnection opens.

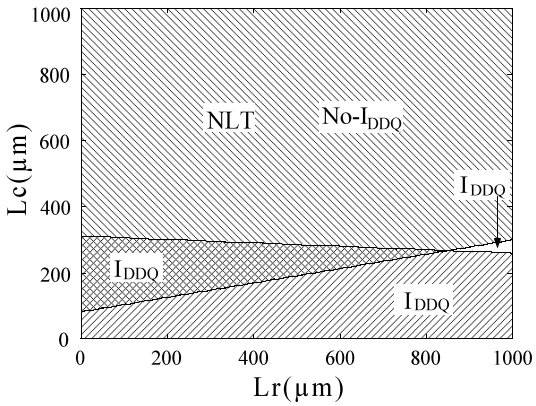


Figure 2.17: Testability regions of interconnection opens for metal 4 for the low controllability case. Line spacing = 3 lambdas

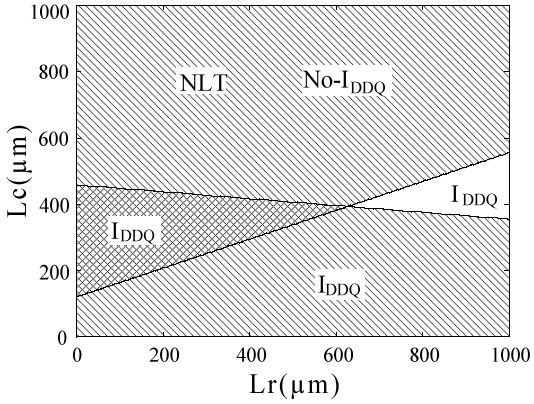


Figure 2.18: Testability regions of interconnection opens for metal 4 for the low controllability case. Line spacing = 5 lambdas

The required line spacing to make I_{DDQ} testable some interconnection opens laid-out in metal 4 non detectable by either I_{DDQ} or a stuck-at based testing are shown in Table 2.2. These opens can not be make logic testable rather the line spacing value.

The required line spacing to achieve detectability of the previous interconnection opens could be too large for some cases (See Table 2.2). Other alternative technique is to place a shield line between the line under test and the coupling adjacent line. This is similar to shielding used to improve testability of bridging faults [78]. The shielding line is biased to V_{DD} (1 logic) or G_{ND} (0 logic) depending on which condition make the open testable. Furthermore, using this second technique even some of the interconnection opens non detectable by either I_{DDQ} or a stuck-at based testing (See Figure 2.14) can became logic testable.

$L_r(\mu m)$	$L_c(\mu m)$	line spacing (lambdas)
350	350	7
600	350	5
700	450	6
800	350	4
800	800	8

Table 2.2: Required line spacing to make I_{DDQ} testable some interconnection opens non detectable by either I_{DDQ} or a stuck-at based testing. Opens located in metal 4.

2.6 Influence of unsensitized gates

In this section, it is investigated the detectability conditions for interconnection opens considering that not all the gates affected by the open are sensitized. Modifications to the proposed capacitive coupling model for interconnection opens are considered. Then, the testability regions considering unsentized gates are determined.

2.6.1 Topology of an unsensitized gate

Unsensitized gates can appear as a consequence of the applied input vector. Due to the unsensitized gates the voltages at the drain/source terminals of the transistors of the affected gates are unknown for the actual input vector. This impacts the charge at the gate of the affected transistors. Hence, the detectability regions of the interconnection opens are also impacted.

The effect of sensitized and unsensitized gates is shown Figure 2.19. Four gates are affected by the interconnection open. Two of them, inverter and Nor gates, are sensitized by the input vectors. However, the two Nand gates (See Figure 2.19) remain unsensitized for the applied input vector.

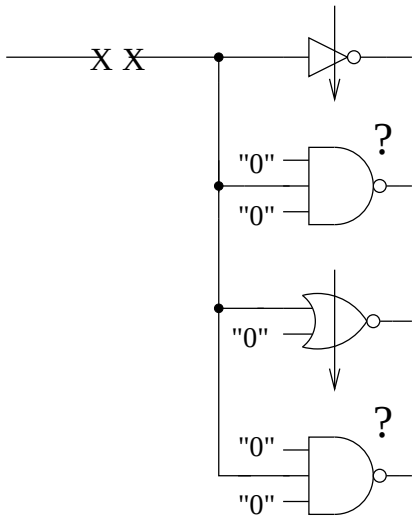


Figure 2.19: Sensitized and unsensitized gates.

For the sensitized gates the power supply and ground are connected through the defective transistors (See Figure 2.20a). Analytical expressions are used to determine the testability regions of interconnection opens. These regions are defined by two voltages at the floating node (V_{if}): a) V_{if}=V_{TN}, and b) V_{if}=$V_{DD} - |V_{TP}|$. For sensitized gates, using the two previous conditions it can be known the voltages at the drain/source terminals of the transistors affected by the open. Using this, the charge of the floating transistors are estimated.

For unsensitized gates, the voltages at the drain/source terminals may depend on the history of the gate. This is shown in Figure 2.20b for a three input Nand gate. The voltage at node V_X can not be determined by the actual input vector.

A schematic representation of a CMOS circuit with transistors affected by the open is given in Figure 2.21. The Nmos and Pmos networks can be composed of series/parallel connected transistors. It is assumed that the input vectors do not sensitize the open. Because this, the voltages at the drain/source terminals of the transistors affected by the open are unknown. These conditions will be considered in the proposed capacitive model of the interconnection open. The resulting topology is shown in Figure 2.21.

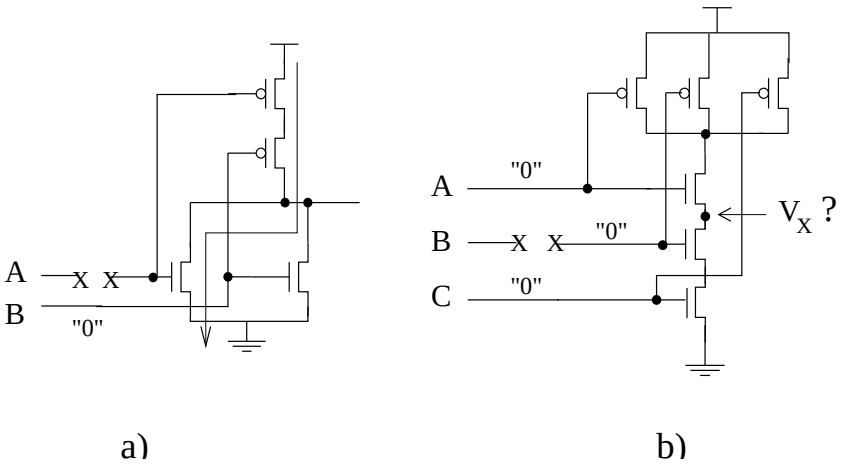


Figure 2.20: Example of sensitized and unsensitized gates.

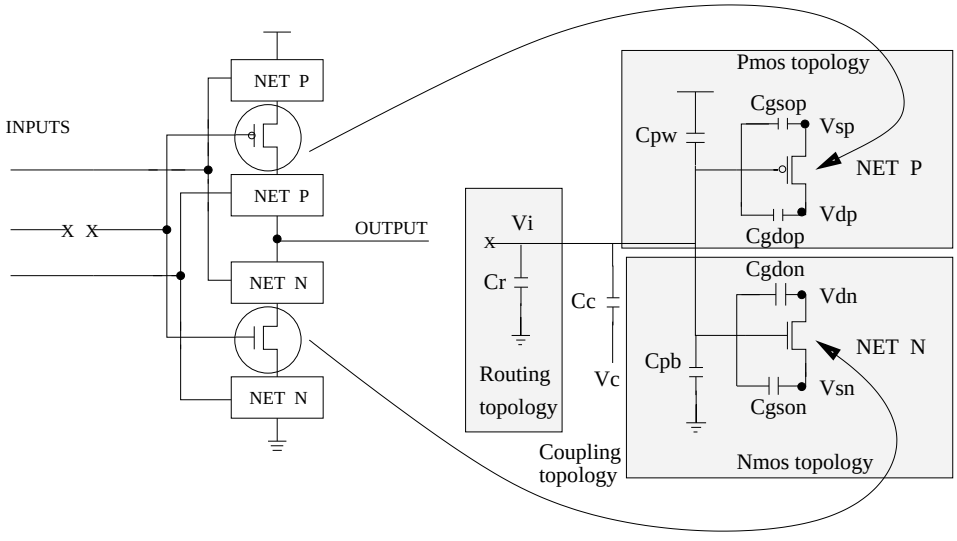


Figure 2.21: Capacitive model for a Pmos, Nmos general unsensitized network.

2.6.2 Testability regions

The testability regions considering the modified capacitive model are determined. According to the law of charge conservation at the floating node, the following equation must be satisfied:

$$\begin{aligned} Q_{tr} &= N_{us}(Q_{GTN} + Q_{GTP} + Q_{Cgson} + Q_{Cgdon} + Q_{Cgdop} + Q_{Cgsop}) \\ &\quad + Q_{Cpw} + Q_{Cpb} + Q_{Cc} + Q_{Cr} \end{aligned} \tag{2.8}$$

where N_{us} is the number of unsensitized gates affected by the open. The other terms have been defined in Section 2.2. Equal sized transistors are assumed. However, the model can be extended to different sized transistors.

Q_{gtn}, Q_{gtp}, Q_{Cgson}, Q_{Cgdon}, Q_{Cgdop} and Q_{Cgsop} are depending on the voltage of the gate, the drain and the source transistor terminals:

$$Q_{gtn}, Q_{gtp}, Q_{Cgson}, Q_{Cgdon}, Q_{Cgdop}, Q_{Cgsop} = f(V_{DN}, V_{SN}, V_{DP}, V_{SP}, V_{if})$$

where charge terms are calculated as the product of the capacitance and the voltages at their terminals.

Replacing the charge terms in equation 2.8, an expression to estimate the voltage at the floating node due to unsensitized gates has been obtained:

$$V_{if} = \frac{V_c C_c + V_{DD} C_{pw} + N_{us}(-Q_{GT} + V_{sn} C_{gson} + V_{dn} C_{gdon} + V_{sp} C_{gsop} + V_{dp} C_{gdop})}{C_{Tus}} \tag{2.9}$$

where:

Q_{GT}=$Q_{gtn} + Q_{gtp}$

C_{Tus}=$N_{us}(C_{gson} + C_{gdon} + C_{gsop} + C_{gdop}) + C_{pb} + C_r + C_c + C_{pw}$

V_c is the voltage at the neighbor line, V_{sn} is the Nmos transistor source voltage, V_{dn} is the Nmos transistor drain voltage, V_{sp} is the Pmos transistor source voltage, and V_{dp} is the Pmos transistor drain voltage.

In the previous equation, it has been considered only the effect of unsensitized gates. Using the previous equation the testability regions for unsensitized gates can be obtained. Transistor threshold voltages (V_{TN}, $V_{DD} - |V_{TP}|$) have been considered as the reference to determine faulty / fault-free behavior at the floating node when the value of the signal at the adjacent coupling line is either V_{DD} or V_{GND}. The same four testability regions obtained for sensitized gates in section 2.4 have been developed for unsensitized gates.

- Guaranteed V_{TN} with C_c at V_{DD}

$$C_r^* \geq \frac{V_{DD}(C_{pw} + C_c) + N_{us}(CV - Q_{GT}) - V_{TN}(C_{Tx})}{V_{TN}} \tag{2.10}$$

where $C_{Tx} = N_{us}(C_{gson} + C_{gdop} + C_{gsop} + C_{gdop}) + C_{pb} + C_c + C_{pw}$

$CV = V_{sn}C_{gson} + V_{dn}C_{gdon} + V_{sp}C_{gsop} + V_{dp}C_{gdop}$

- Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{DD}

$$C_r^* \leq \frac{V_{DD}(C_{pw} + C_c) + N_{us}(CV - Q_{GT}) - (V_{DD} - |V_{TP}|)(C_{Tx})}{V_{DD} - |V_{TP}|} \tag{2.11}$$

- Guaranteed V_{TN} with C_c at V_{GND}

$$C_r^* \geq \frac{V_{DD}C_{pw} + N_{us}(CV - Q_{GT}) - V_{TN}(C_{Tx})}{V_{TN}} \tag{2.12}$$

- Guaranteed $V_{DD} - |V_{TP}|$ with C_c at V_{GND}

$$C_r^* \leq \frac{V_{DD}C_{pw} + N_{us}(CV - Q_{GT}) - (V_{DD} - |V_{TP}|)(C_{Tx})}{V_{DD} - |V_{TP}|} \tag{2.13}$$

The developed expressions for the unsensitized gates are combined with the expressions for the sensitized gates. The resulting expression is used to determine testability regions for interconnection open. As a first approach, it has been assumed that the uncertainty voltages (V_{sp}, V_{dp}, V_{dn}, V_{sn}) can have extremal values of 0V and V_{DD}. Four gates are affected by the open. All the gates are equally sized. The following cases are considered:

Gates	Case A	Case B	Case C
Sensitized	1	2	3
Unsensitized	3	2	1

Table 2.3: Analyzed cases for unsensitized gates.

The testability regions are obtained for the full controllability case. It is considered that floating routing line runs over the substrate. The effect of the initial trapped charge is not taken into account.

The testability regions for the case of three sensitized gates and one unsensitized are shown in Figure 2.22. It can be observed that a band appears in the borders delimiting the testability regions. Because the presence of the unsensitized gate, it can not be assured that either logic testing or I_{DDQ} testing detect opens with these defect topology parameters (C_r, C_c). However, these opens will be detected by any of the two test techniques. The uncertainty band is wider when the number of unsensitized gates increases. This can be observed in Figures 2.23 and 2.24, where the number of unsensitized gate is two and three, respectively.

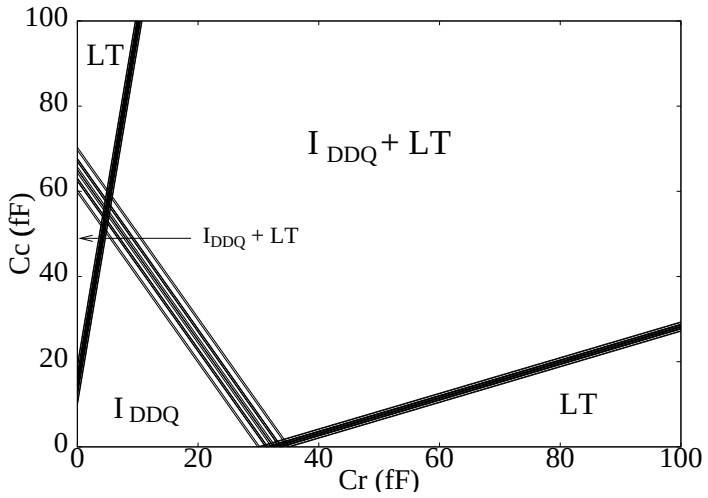


Figure 2.22: Sensitized gates=3, unsensitized gates=1.

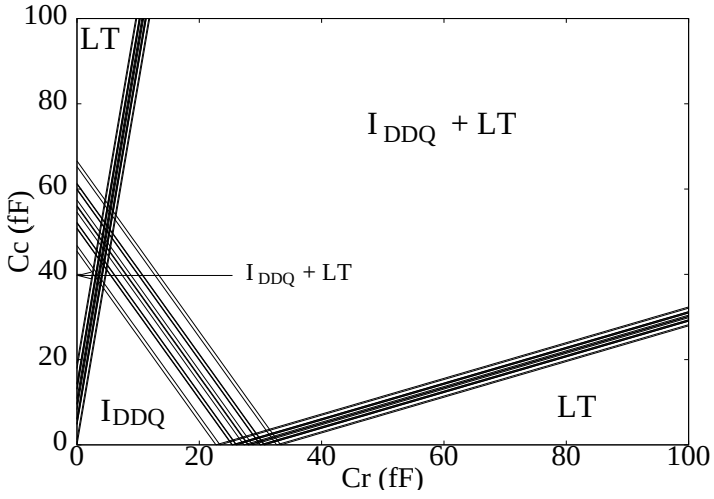


Figure 2.23: Sensitized gates=2, unsensitized gates=2.

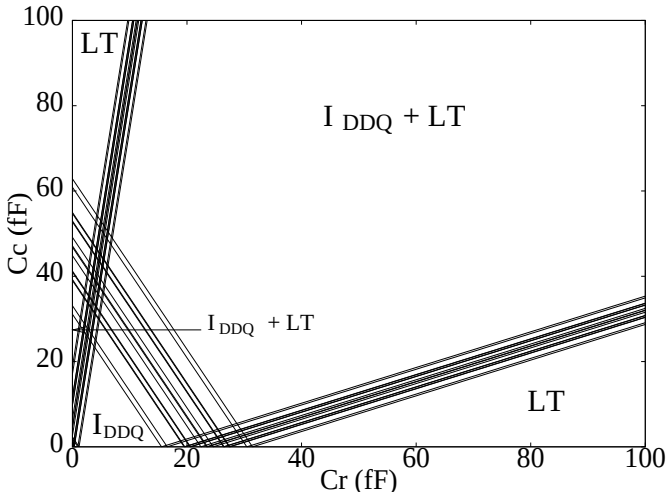


Figure 2.24: Sensitized gates=1, unsensitized gates=3.

2.7 Experimental measurements

Inverters intentionally designed with interconnection opens have been manufactured. The dependency of the behavior of interconnection opens on the defect topology parameters is illustrated. The structures have been designed using ES2's Dual Layer Metal, 1.5μm, n-Well CMOS Technology. A photograph taken with a microscope of a designed inverter with an interconnection open is shown in Figure 2.25. The gate of the defective inverter is not connected to any control signal.

The measurements have been made at room temperature (25 °C) with dark lights using an HP4145B Semiconductor Parameter Analyzer. In Figure 2.26, $C_{V_{GND}}$ ($C_{V_{DD}}$) represents the sum of all capacitances with one terminal connected to the floating node and the other to V_{GND} (V_{DD}).

- For a defective inverter designed with $C_{V_{GND}}$=3.8fF and $C_{V_{DD}}$=23.8fF, the output voltage is at a well-defined low logic level (curve 1 in Figure 2.26). This behavior is due to the high value of $C_{V_{DD}}$. The estimated equivalent induced gate voltage from the experimental data is 2.55V.

- A second inverter was designed with $C_{V_{GND}}$=3.8fF and $C_{V_{DD}}$=3.8fF. The output voltage increases for this defective inverter (curve 2 in Figure 2.26). This is because the induced gate voltage decreases for lower values of $C_{V_{DD}}$.

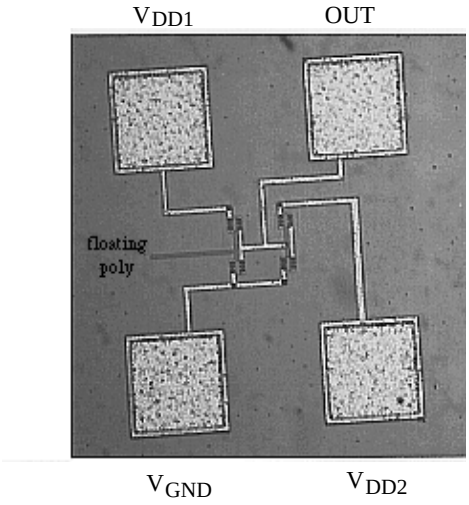


Figure 2.25: Photograph of a designed inverter with an interconnection open. The input of the inverter is not connected to any driving signal.

Consequently, the output voltage increases. The estimated equivalent induced gate voltage from the experimental data is 2V.

- A third inverter was designed with $C_{V_{GND}}$=23.8fF and $C_{V_{DD}}$=3.8fF. The output voltage increases due to the higher $C_{V_{GND}}$ value (curve 3 in Figure 2.26). An intermediate voltage appears for this case so the logical behavior of the defective inverter cannot be assured. This in turn will depend on the threshold gate voltage of the load gate. The estimated equivalent induced gate voltage from the experimental data is 1.87V.

Similar experimental results to those presented above have been found by Hawkins et al. [54]. They have measured voltages at the floating node and output voltages which depend on the open location.

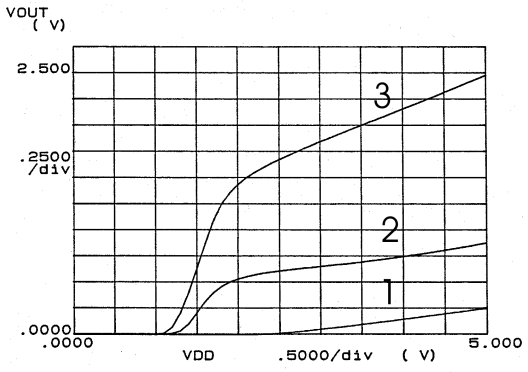


Figure 2.26: Measured output voltage in defective inverters for different interconnection open defects, W_P=W_N=15.2μm. 1: $C_{V_{GND}}$=3.8fF $C_{V_{DD}}$=23.8fF, 2: $C_{V_{GND}}$=3.8fF $C_{V_{DD}}$=3.8fF, 3: $C_{V_{GND}}$=23.8fF $C_{V_{DD}}$=3.8fF.

2.8 Conclusions.

The most important results obtained in this chapter are:

- The detectability of full interconnection opens by logic and I_{DDQ} testing has been investigated.
- A coupling capacitive model has been proposed for interconnection opens. This model takes into account technology and topology parameters. The defect location introduces two important parameters: a) the floating routing capacitance, and b) the capacitances coupled to the defective line.
- Explicit analytical expressions have been developed to determine the testable regions of interconnection opens.
- It has been found that the detectability of interconnection opens is strongly dependent on the signals coupled to the defective one. Three cases have been considered: a) full controllability, b) partial controllability, and c) low controllability.
- High coverages of interconnection opens can be obtained using both I_{DDQ} and a stuck-at based testing methodologies for the full controllability case. Furthermore, the relative efficiency of each testing approach also depends

on the metal layer where the signal are laid-out. It was found that stuck-at based testing works better in lower metal levels while I_{DDQ} testing performs better in upper metal levels.

- The efficiency of a stuck-at based testing decreases for the case of partial controllability.

- Some interconnection opens non detectable by either a stuck-at based or I_{DDQ} testing appear for the case of low controllability. This situation occurs when the most favorable stuck-at vectors for an interconnection open can not be generated due to the topology of the circuit. Routing design for testability techniques should be used in order to make detectable this type of opens.

- The effect of unsensitized gates on the detectability of interconnection opens have been investigated. Due to the unsensitized gates, a range of defect topology parameters appears for which it can not be assured that I_{DDQ} or logic testing detects the defects. Because, this both I_{DDQ} and logic testing should be used for obtaining high coverages of interconnection opens.

- Experimental data showing the influence of the defect topology parameters on the behavior of a defective inverter has been presented.

Chapter 3

Resistive opens in CMOS memory elements.

3.1 Introduction

In this chapter, the behavior of CMOS memory elements in the presence of resistive opens is investigated. Conditions to test resistive opens by logic and delay testing are determined. The obtained results can also be used to enhance actual faults models for CMOS memory elements which can be used for fault simualtion and test pattern generation.

It has been found that some resistive opens could be hard to detect [5] [4]. Needham et al. [5] have found via failures at post-production for Pentium MMX ICs only when the simulated resistance was greater than 830KΩ. They have found that some open defects were detected only when appropriate stress conditions (temperature, voltage, frequency) were applied. Baker et al. [4] have investigated the use of delay testing to test resistive opens. They have found that the resolution of delay fault testing impact the detectability of these defects. In addition, the process parameter variation must be taken into account to define the pass/fail limits [4]. It has been found that stuck-at coverage does not give high coverages of the defects in sequential cells [79]. The behavior and test of resistive opens in CMOS latches have not been widely investigated. Some authors have addressed the case of opens of very high resistance in CMOS latches.

DFT (Design for Testability) techniques have been proposed to test otherwise undetectable opens in certain conducting branches of CMOS latches [80] [81]. Because minimal model faults can not correctly detect faults in storage elements, enhanced models has been proposed by [82]. Champac et al. [83] have analyzed the detectability of floating gate defects in sequential circuits by I_{DDQ} and logic testing. McCluskey et al. [84] have proposed testing latches by checking experiments. They give the conditions for exhaustive functional test. The analysis by checking experiments is not only applicable to latch structures but also for complex structures as flip-flops or scan chains [85] [86] [87]. Ferguson et al. [88] have investigated the testability of opens in a CMOS sequential scan path cell. They have proposed design and layout modifications to reduce the probability of difficult-to-detect faults.

In this chapter, a close analysis of the behavior of resistive opens in CMOS latches and flip-flops is carried-out. The analysis is made for different possible realistic locations of the open. The detectability of the different open locations by logic and delay testing is investigated. Testable latches and flip-flops including DFT structures are proposed for those opens non-detectable by voltage based testing. The influence of charge sharing in the testability of resistive opens in CMOS memory elements is investigated. Symmetric and transmission gate based latches and flip-flops [79] [89] [86] [90] [91] are considered. However, the results can be extended to other static memory cells [90].

This chapter is organized as follows: in Section 3.2, the analysis in the symmetric CMOS D-latch cell is presented. In Section 3.3, the behavior of resistive opens in the transmission gate CMOS latch is presented. In Section 3.4, the analysis is extended to the symmetric flip-flop cell. In Section 3.5, the analysis is extended to the transmission gate flip-flop. In Section 3.6, the timing conditions to test resistive opens in memory elements in a scan path chain are stated. Scan path chains composed by symmetric and transmission gate flip-flops are considered. Experimental measurements are presented in section 3.7. Finally, in Section 3.8 the conclusions of the chapter are given.

3.2 Analysis in the symmetric CMOS D-latch cell

The behavior of the CMOS latch cell in the presence of resistive opens has been investigated. The location of the break is modeled with a lumped resistance which can take a continuous range of values. We use HP 0.35μm, N-Well CMOS technology.

A sequence of two vectors pattern is applied to test the CMOS latch cell (See Figure 3.1):

- A first vector V_1 is applied in order to initialize the latch (0,1). The writing (memory) time is defined by clock at low (high) level.
- A second vector V_2 is applied to toggle the state of the latch (0→1, 1→0).
- The latch output Q is observed a time after the beginning of the memory phase. Fault-free behavior is obtained if the observed data agree with the expected data, in other way the device is faulty.

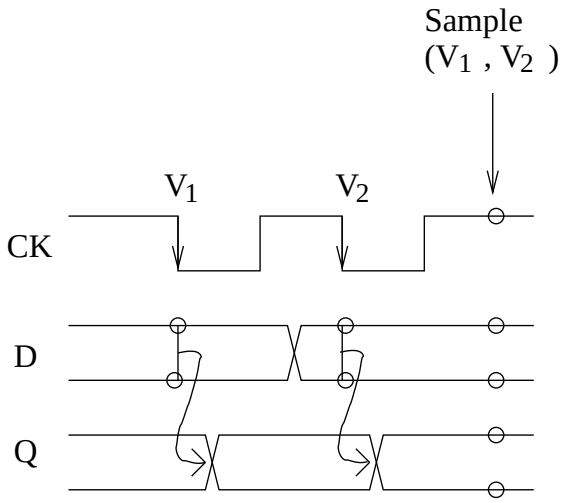


Figure 3.1: Two vector pattern test.

The behavior of the CMOS latch is analyzed varying the time since the data changes (second vector) until the leading edge of the clock (memorizing phase) occurs. This time has been called t_{xsu} (See Figure 3.2). The delay time (t_d)

of the latch is measured for the second applied vector. t_d is the time since the data changes to the time the latch output reaches 90% (10%) of the power supply. The delay time of the latch is not measured at the middle value of the power supply because this can be an unstable region, and for some defects the latch output reaches this value and then switches in the opposite direction. The effect of initial conditions prior to the application of the sequence of the two vectors is also analyzed. This is specially important for high resistive opens where the nodes may not be settled during the application of the second test vector [46].

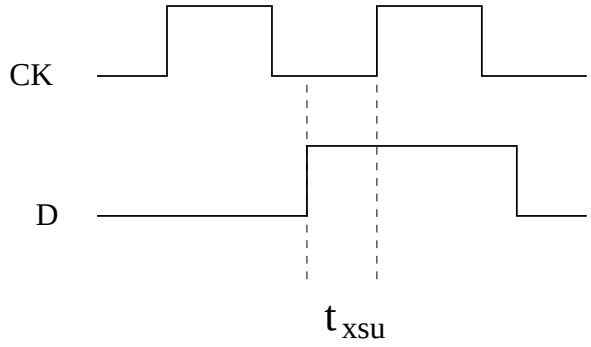


Figure 3.2: Concept of t_{xsu}.

3.2.1 Symmetric CMOS D-Latch Cell

A CMOS latch based on triestable inverters is considered (See Figure 3.3). The symmetric CMOS latch is composed by two clocked triestable CMOS inverters and one static CMOS inverter (output stage). The schematic of the analyzed CMOS latch with all the considered resistive opens is shown in Figure 3.4. The analysis focus in resistive opens affecting the Nmos networks. Opens in the Pmos networks can be analyzed in a similar way. The analysis has been made for resistive opens located in each stage of the latch. Resistive opens in the conducting paths and in gates are analyzed. The opens in gates can affect to one gate or multiple gates.

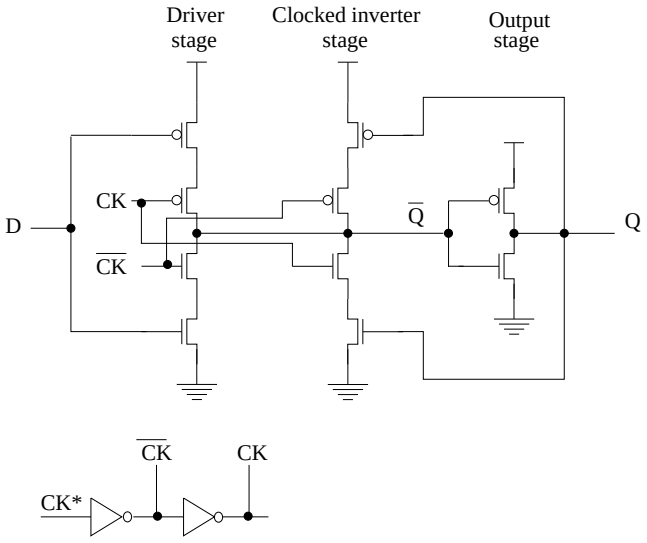


Figure 3.3: Symmetric CMOS latch.

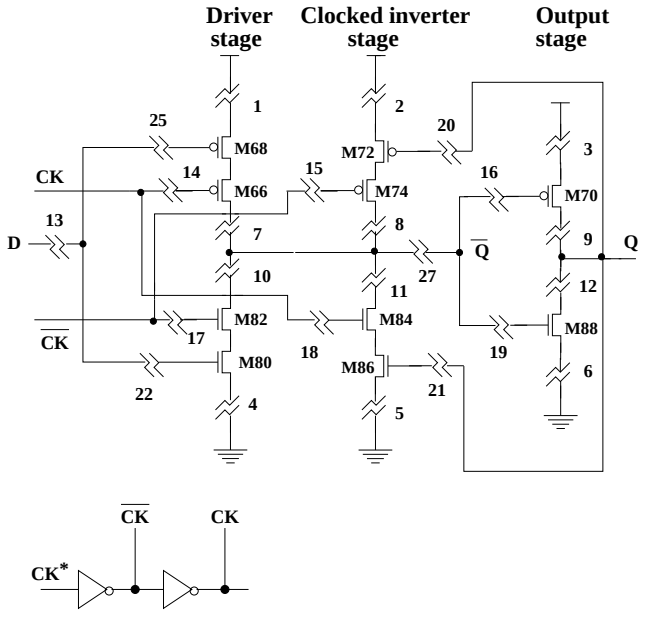


Figure 3.4: Resistive opens in the CMOS latch.

3.2.2 Resistive Opens in the Driver Stage

The possible resistive opens affecting this stage (See Figure 3.4) have been classified as follows:

- Opens in Nmos (Pmos) conducting paths: R_{10}, R_4 (R_7, R_1)
- Opens in gates.- Two cases are found:
  - Multiple open gates: R_{13}
  - Single open Nmos (Pmos) gates: R_{17}, R_{22} (R_{14}, R_{25})

Resistive opens in conducting paths

Resistive opens located in conducting paths increase the delay time of the latch and a logic error may occur under certain timing conditions. Resistive open R_{10} is considered to analyze this case. This open is located in the Nmos network of the driver stage (See Figure 3.4). A two vector test is used to excite the open. The first vector (D=0) initialize the latch output to 0 state (See Figure 3.5). During the writing phase (CK=0) of the second vector (D=1) the voltage at node Q ($\overline{Q}$) increases (decreases) slowly. The latch output takes a long time to switch due to the presence of the open. The final logic state of the latch depends on the values of the voltages Q, $\overline{Q}$ at the beginning of the memorizing phase [83]. For a given resistance of the open, the voltage at the nodes Q, $\overline{Q}$ at the beginning of the memorizing phase depends on the time t_{xsu}. In the case shown in Figure 3.5, the defective latch cell memorizes incorrectly the input data.

In Figure 3.6 the delay time at the CMOS latch output for different t_{xsu} for open R_{10} is shown. For a given resistance of the open, the output of the CMOS latch is able to reach its final correct logic state for sufficient large values of t_{xsu}. Furthermore, the delay time of the defective CMOS latch increases respect to the fault-free case (See Figure 3.6). As t_{xsu} is decreased but still large enough, the delay time does not depend on the value of t_{xsu}. However, for a sufficient small value of t_{xsu}, the delay time increases as t_{xsu} decreases. This is because when the memorizing phase starts the latch is close to the metastability state. The delay time increases for a larger value of the resistance of the open. For a certain low value of t_{xsu} (dark circle in Figure 3.6) the CMOS latch will not operate logically

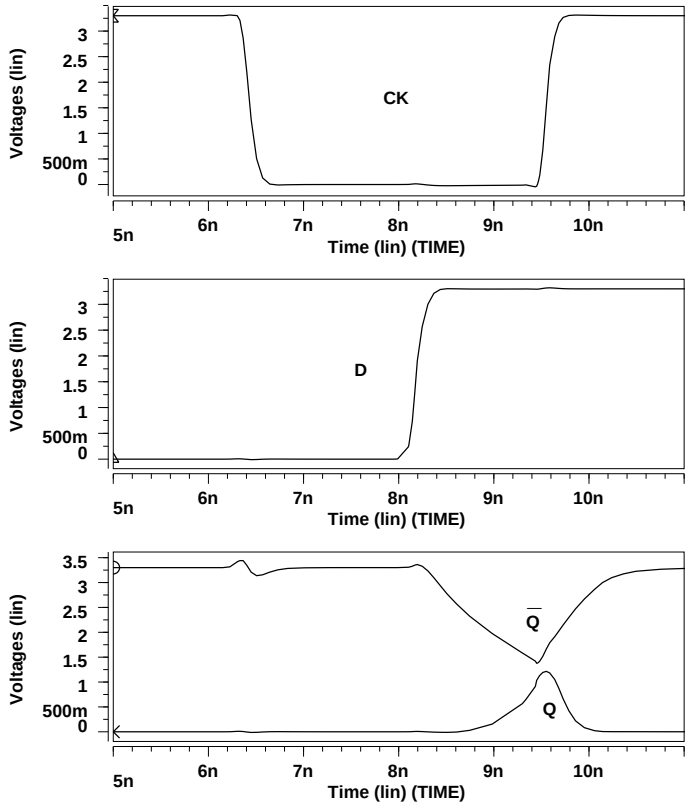


Figure 3.5: Timing diagram for resistive open R_{10}.

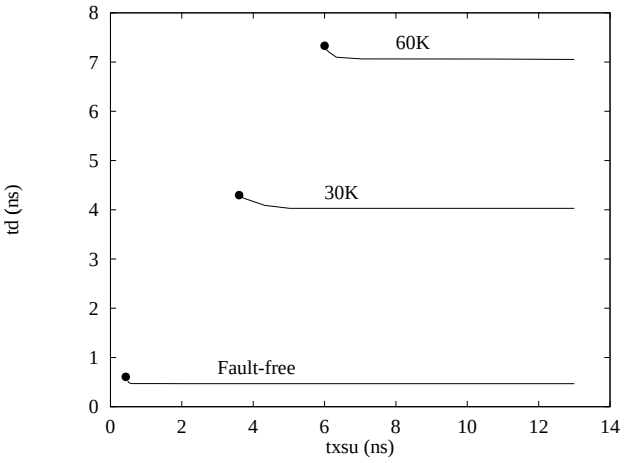


Figure 3.6: t_{delay} for resistive open 10

correctly. These results indicate that resistive open R_{10} may be detected by delay based testing and a logic error may appear under certain timing conditions. The actual minimum detectable resistance of the open depends on the process variation [4].

Resistive opens in gates

Resistive opens in gates deserve particular attention. A significant range of these opens can be detected using a sequence of two vectors [92]. However, the detectability of high resistive opens depends strongly on the initial conditions prior to the application of the sequence of two vectors. The gate(s) of the affected transistor(s) may acquire an initial voltage condition (V_{ic}) depending on the history of the gate.

- Multiple open gate

Resistive open R_{13} is considered (See Figure 3.4). Either the 0→1 or 1→0 input data transitions can be applied to excite this open. The detectability conditions of a significant range of resistive opens located in this position is similar to opens in conducting paths (See Figure 3.7). The delays are smaller (See Figure 3.7) to those found in opens in conducting paths (See Figure 3.6).

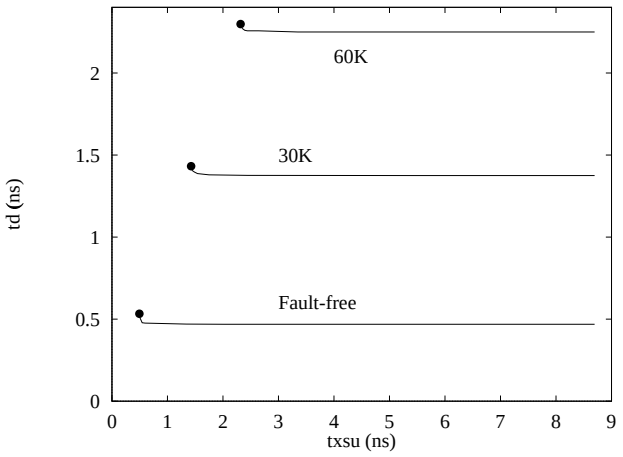


Figure 3.7: t_{delay} for resistive open 13

The detectability of high resistive opens depends on the initial voltage condition at the gates of the affected transistors (M80 and M68 in Figure 3.4). Intermediate initial voltage conditions could produce that the affected Nmos and Pmos transistors are partially conducting. The delay time for the two possible input data transitions is given in Figure 3.8.

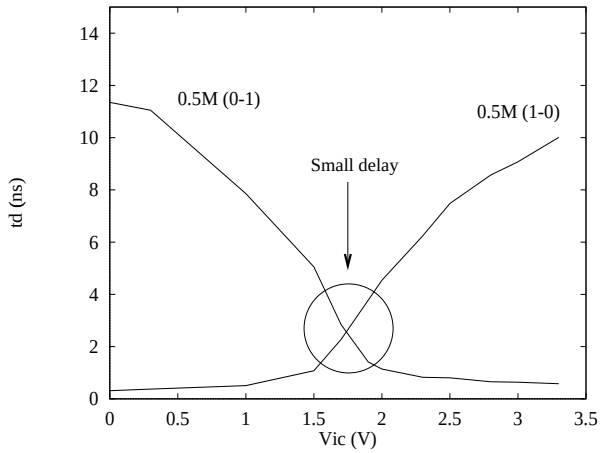


Figure 3.8: t_{delay} for resistive open 13 for high resistive opens.

For 0→1 transition and low voltages as initial conditions, the delay increases significantly because the initial voltage condition tries to write a 1 logic instead of a 0 logic (for the second vector). Low initial conditions, higher than the threshold voltage of the Nmos transistor, create a competition between the Nmos and Pmos network of the driver inverter. Then, the node to the right of the resistive open is slowly charged-up according to the input data. As a consequence the delay time increases. The delay is larger when the initial conditions are lower than the threshold voltage of the Nmos transistor. For this open location, high voltages as initial condition means that the first vector of the sequence 0→1 failed. Hence, the defect can be detected monitoring the latch output for every clock cycle (for the first and second vector). In other words this means that the latch is failing for the other input transition. However, high resistive opens with intermediate voltages around $V_{DD}/2$ as initial condition can not produce a logic error. Furthermore, these opens produce small delays (See Figure 3.8). Hence, they could not be detected by neither a logic based testing or a delay based testing. The 1→0 transition has a similar behavior to the 0→1 transition. A possible strategy

to test these opens with initial conditions around $V_{DD}/2$ is to apply a longer cycle time for the first initialization vector. Or to add a pause time prior to the two test vector sequence. In this way, initial voltage condition goes away from the $V_{DD}/2$ region. As a consequence the delay increases or a logic error can appear.

- Single open gates

For this case, resistive opens R_{17} and R_{22} are analyzed. Let's consider first resistive open R_{17} (See Figure 3.4). This open is only affected by the 0→1 transition. The 1→0 transition does not have influence on this open because the lower Nmos transistor (M80) in the driver stage (See Figure 3.4) is turned-off for the second vector. For the 0→1 transition, the delay also increases for low resistive opens as in the previous case. For high resistive opens, the detectability of the defect depends on the value of the initial voltage condition. High resistive opens are detectable for low voltages of initial conditions (See Figure 3.9).

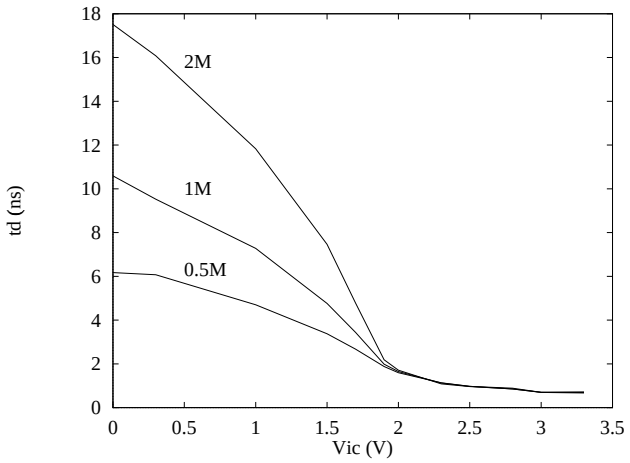


Figure 3.9: t_{delay} for resistive open 17. 0→1 transition.

This is because for low initial conditions the transistor M82 initially turned-off or conducting weakly. For the second vector (D=1), the gate of the defective transistor (M82) is slowly charged-up through the open resistance. As a result large delays appear. However, high resistive opens are not detected for high voltages as initial conditions (See Figure 3.9). High resistive opens with high values

of initial conditions (See Figure 3.9) could be hard to detect. A very long pause time could be required for these opens in order to have significant delay values (See Figure 3.9). This could increase significantly the test time.

Let's consider now resistive open R_{22}, this open can be excited by transition 0→1 and 1→0 at the input data. The delay increases depending on the transition and the value of the initial voltage condition (See Figure 3.10). For this open location it is less likely that the first vector of the two pattern sequence fails (like in R_{13}). This is because the complementary transistor to that affected by the open receives correctly the input data.

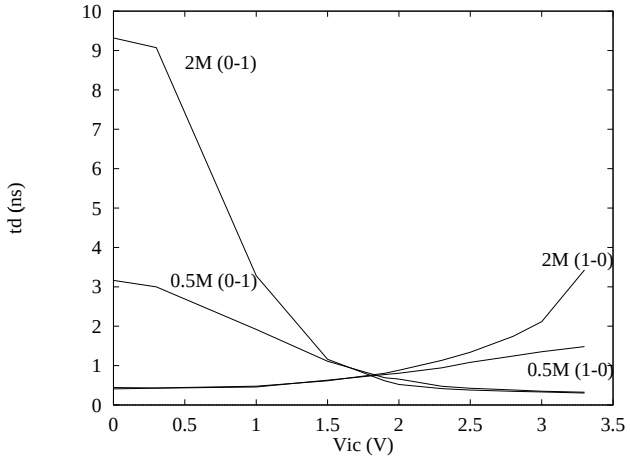


Figure 3.10: t_{delay} for resistive open 22.

3.2.3 Resistive Opens in the Output Stage

The opens in the output stage are also classified in a similar way to the opens in the driver stage: a) Opens in Nmos (Pmos) conducting paths: R_6, R_{12} (R_9, R_3), b) Opens in single Nmos (Pmos) open gates: R_{19} (R_{16}) and c) Multiple open gates R_{27}.

The behavior and conditions to test these opens are similar to those opens in the driver stage. The delay increases significantly for opens located in conducting paths but the latch is able to reach its final correct logic state for sufficient large values of t_{xsu} times. However, as t_{xsu} time decreases it could be possible that the

CMOS latch does not operate logically correctly and logic error is produced so the open is detected. High resistive opens in gates are also influenced by initial voltage conditions.

3.2.4 Resistive Opens in the Clocked Inverter Stage

The opens in this stage are classified as follows:

- Opens in Nmos (Pmos) conducting paths R_5, R_{11}, (R_8, R_2)
- Opens in the control path R_{18} (R_{15})
- Opens in the feedback path R_{21} (R_{20})

Opens in conducting paths

For opens in conducting paths, the input data is correctly written and memorized. Non significant delay increment is appreciated at the output of the CMOS latch. These opens can not be detected by either logic or delay testing. However, for very high resistive opens the latch fails to retain the information after some time in the presence of leakage or noise [93] [94] [88]. A data retention test can be used to test these opens. This approach is expensive in terms of test time. DFT solutions for very high resistive opens have been proposed [80] [81]. In the next subsection, DFT proposals to test resistive opens in conducting paths of the clocked inverter stage are proposed.

Opens in the control path

The latch is able to write and memorize correctly the input data in the presence of these opens. Furthermore, non significant delay increment is observed at the CMOS latch output. Hence, delay testing is not able to detect these opens. A data retention test [94] [93] may be used to test high resistive open in the control path. Layout techniques (e.g. increasing the number of contact and/or vias) may also be used to reduce the probability to occur of these opens [95].

Opens in the feedback path

Opens located in this position are not detectable by either logic or delay testing for a wide range of values of resistance of the open. However, the behavior of the defective latch cell, for high resistive opens, depends on the initial voltage condition.

For resistive open R_{21} (See Figure 3.4), the transition 1→0 is applied to the input D. For the second vector (D=0), the input data is initially correctly written and memorized at the output of the CMOS latch (See Figure 3.11).

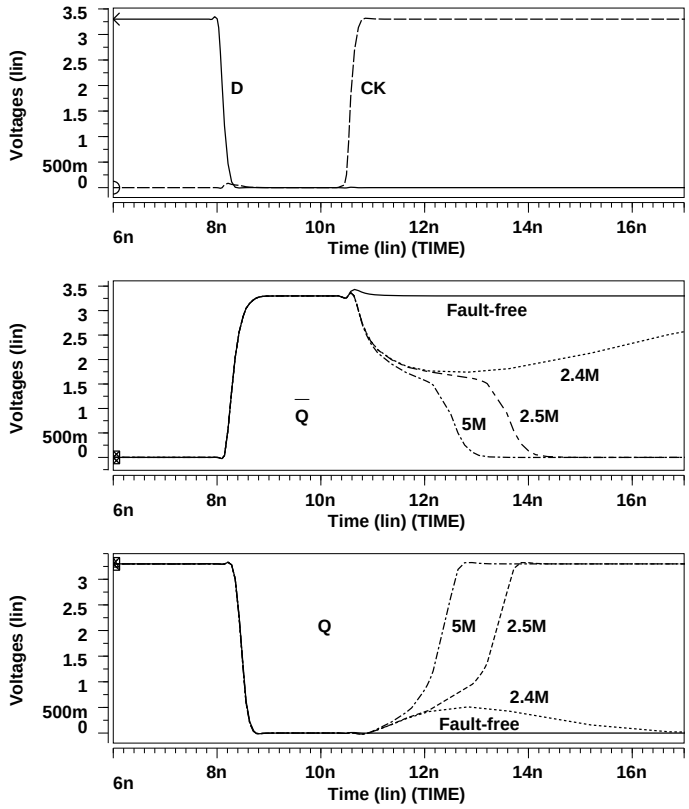


Figure 3.11: Timing diagram for resistive open R_{21}

There is non significant delay increment. However, the output of the CMOS latch may flip to the wrong state for sufficiently very large resistance value of the open and high values of the initial voltage condition. This behavior is because

the transistor affected with the open is "on" when the memorizing phase starts for a high resistive open. This produces a competition between the strengths of the Pmos and Nmos networks of the clocked inverter stage (See Figure 3.12). If the initial voltage at the gate of the defective transistor is high enough then it could be possible that Nmos network wins the competition.

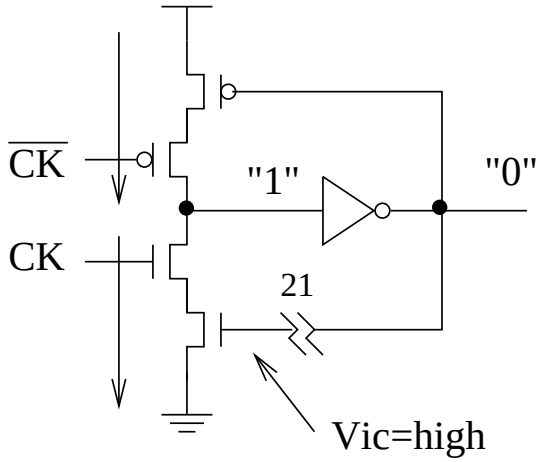


Figure 3.12: Networks competition for resistive open R_{21}

The time for an error to appear at the latch output (t_{error}) has been measured since the clock changes the latch to memory until the latch output reaches 90% of V_{DD} (See Figure 3.13). It should be noted that a traditional delay testing can not detect these opens. A sufficient time must be waited for sampling the CMOS latch output. The detectable resistive opens are in the order of Megaohms (See Figure 3.13). Lower values of resistive opens are not detectable by delay testing. The output of the CMOS latch behaves correctly for low values of resistive opens. However, large resistive opens produce a data retention fault or a logic error.

For a data input D=1, the latch is also able to write and memorize correctly the data. However the node $\overline{Q}$ floats for initial voltage conditions lower than the threshold voltage of the transistor M68 (See Figure 3.4). The final state of the latch depends on the winner of two mechanisms: a) charging-up of the gate of affected transistor through the open resistance, and b) leakage of the floating node $\overline{Q}$.

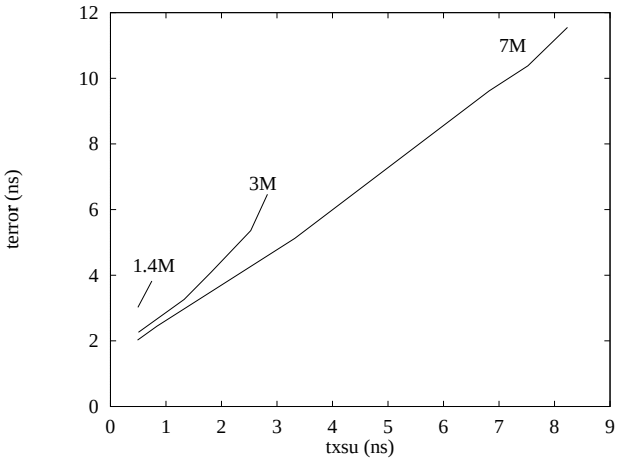


Figure 3.13: t_{delay} for resistive open 21.

3.2.5 A DFT Testable Latch Cell

It is well known that full-opens (stuck-opens) in conducting paths in the clocked inverter are undetectable by traditional voltage based testing techniques [80] [81]. The input data is correctly written and memorized but the information may be lost due to leakage or noise. DFT approaches have been proposed to make detectable these branches for full-opens [80] [81] [92].
In this subsection two DFT CMOS latch cells to test resistive opens in conducting paths of the clocked inverter stage are proposed:

- DFT testable latch with two control signals
- DFT testable latch with one control signal

DFT testable latch with two control signals

In this proposal [92], two additional transistors and two control signals are required (See Figure 3.14). M_{TP} (M_{TN}) DFT transistor is activated when resistive opens in the Nmos (Pmos) network are required to test. A competition between Nmos (Pmos) network and M_{TP} (M_{TN}) determines if the conducting path of the clocked inverter stage is faulty or fault-free.

For this DFT technique only one DFT transistor is activated. When the Pmos transistor of the DFT circuit is activated the Nmos transistor is disactivated and

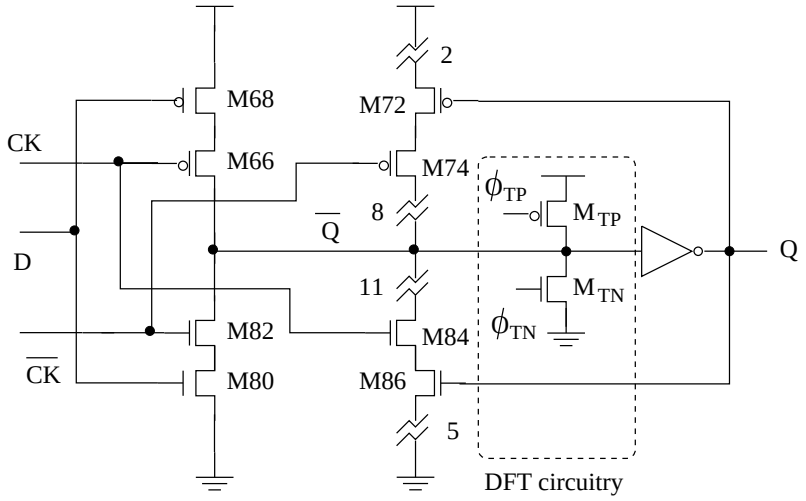


Figure 3.14: Memorizing circuit with the two DFT transistors.

viceversa. Resistive opens in the Nmos (Pmos) network are tested as follows:

- Initialize the latch to 1 (0) state.
- In memory phase, activate Pmos (Nmos) transistor M_{TP} (M_{TN}).
- Disactivate Pmos (Nmos) transistor M_{TP} (M_{TN}).
- Observe the output of the CMOS latch.

Nodes Q and $\overline{Q}$ evolves to a stable quiescent state after M_{TP} (M_{TN}) transistor is disactivated. The Pmos transistor M_{TP} (M_{TN}) is sized such that the defective latch flip its state but the fault-free latch remains unchanged.

Let's analyze resistive open R_{11} in the Nmos network (See Figure 3.14). The initialized state is given at the beginning of the Figure 3.15. During the activation phase (ϕ_{TP}=0), the voltage at the node Q ($\overline{Q}$) decreases (increases). Resistive opens equal or higher than 18KΩ flip the state of the CMOS latch. Hence, these opens are detected. Resistive opens lower than 18KΩ do no change the state of the latch. Hence, these opens are not detected.
The minimum detectable resistance value of the open is determined by the width of the activation signal (T_{WT}) and the channel width of the Pmos transistor M_{TP}. The previous conditions are chosen to flip the state of the defective CMOS latch.

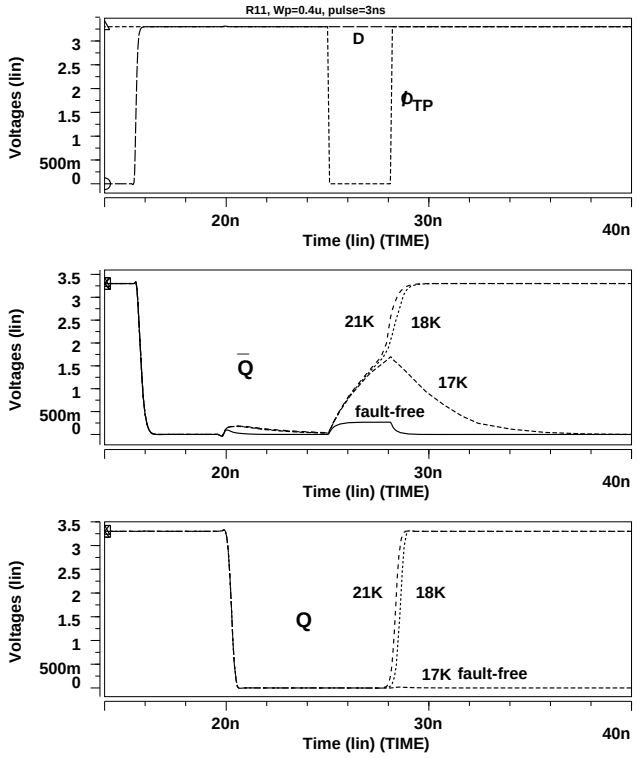


Figure 3.15: Timing diagram for DFT circuitry. Resistive open R_{11}, W_P^*=3μm.

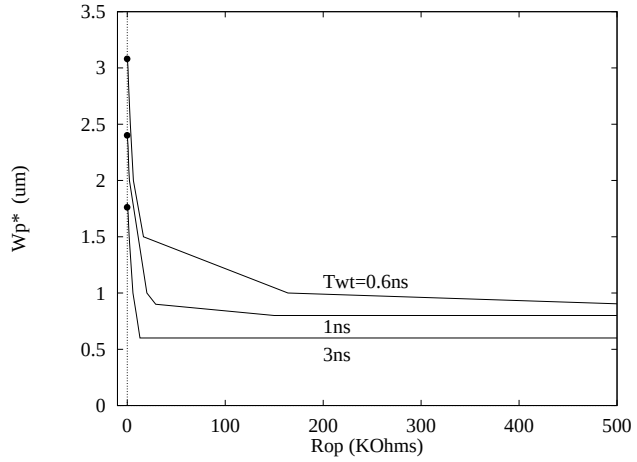


Figure 3.16: Minimum channel width of M_{TP} (W_P) for detecting a given open. T_{WT} is the width of the activation signal.

At the same time, the fault-free CMOS latch must not change its state.

The required conditions to detect resistive opens in the CMOS latch are given in Figure 3.16. W_p^* is the minimum required channel width of the Pmos transistor to detect a given resistive open. The maximum allowed channel width of the transistor M_{TP} is shown with a dot in Figure 3.16. Larger channel widths of M_{TP} also flip the state of the fault-free CMOS latch. It can be seen that a wider time of the activation signal requires a smaller M_{TP} transistor. The cost of the proposed approach has been estimated in terms of speed degradation and area (See Table 3.1).

$W_p^*(\mu\text{m})$	R_{Min}^{Det}	$\Delta T_d\%$	$\Delta A\%$
1.2	6.5MΩ	1.30 (14ps)	2.0
3.0	5.0KΩ	2.15 (23ps)	3.4

Table 3.1: Cost of the DFT. T_{WT}=10ns

ΔT_d is the speed penalty (writing time) of the latch with the DFT transistors respect to the case without DFT circuitry. In a similar way, ΔA is the area penalty. R_{Min}^{Det} is the value of the minimum detectable resistance. The actual value of W_P^* for R_{Min}^{Det} must be chosen taking into account the process corners. As can be seen in Table 3.1 the addition of the two DFT transistors do not degrade significantly the dynamic characteristics of the CMOS latch.

At system level routing of two control signals is required. This impacts the area. At global circuit level, the additional inputs can be used for all the memory elements. Additional routing also means addition of capacitance, and hence power consumption. It is expected a minimal impact on the power consumption during test mode. This is because the control signals are put in one state an then they are kept constant. During normal operation the control signals are kept constant. Power consumption increases slightly due to the added capacitance in the memory element by the DFT transistors.

DFT testable latch with one control signal

A second DFT approach for memory elements using only one control signal has been proposed for reducing the cost of routing and extra pins. For this DFT proposal, four additional transistors and only one control signal are required (See Figure 3.17). Both DFT transistors M_{TP} and M_{TN} are activated at the same time to test resistive opens in the Nmos/Pmos networks. The network under test (Nmos or Pmos) is selected by the initialized state of the latch.

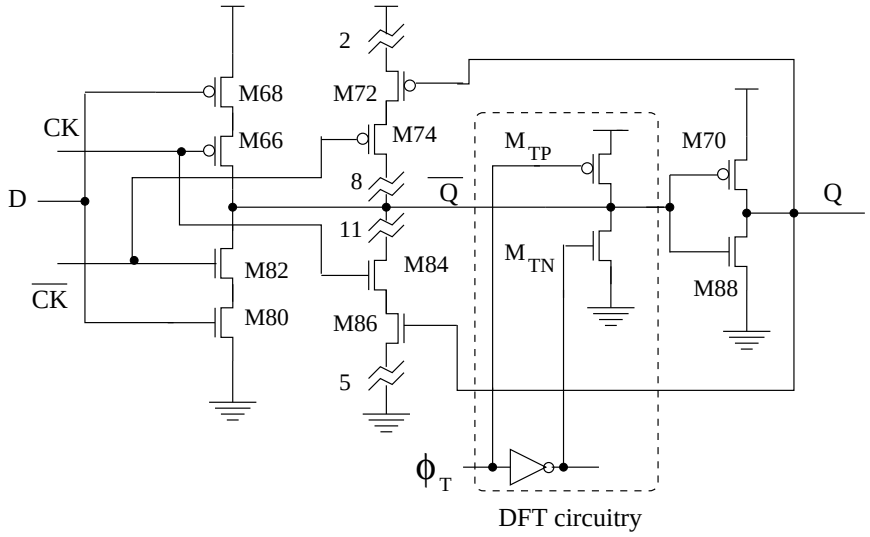


Figure 3.17: Proposed Testable Latch with one control signal.

Resistive opens in the Nmos (Pmos) network are tested as follows:

- Initialize the latch to 1 (0) state.
- In memory phase, activate transistors M_{TP} and M_{TN}.
- Disactivate both transistors M_{TP} and M_{TN}.
- Observe the output of the CMOS latch.

Let's consider a resistive open in the Nmos network (See Figure 3.18a). The latch output is initialized to 1 state. When the two test transistors M_{TP} and M_{TN} are activated there is a competition of three networks: the Nmos conducting path, M_{TP} transistor and M_{TN} transistor (See Figure 3.18 a). Due to the

resistive open the strength of the Nmos network of the clocked inverter decreases. Hence, different intermediate voltages at Q and $\overline{Q}$ appear for the fault-free and the defective cases. Once the transistors M_{TP}, M_{TN} are disactivated the cell evolves to a stable quiescent state. The transistors M_{TP} and M_{TN} are sized such that the defective latch flip its state but the state of the fault-free latch remains unchanged. The opposite is true for resistive opens in the Pmos network (See Figure 3.18b). The actual behavior of the CMOS latch with the DFT transistors is similar to the weak write test mode proposed by Meixner et al. [96] for data retention faults in CMOS SRAMs.

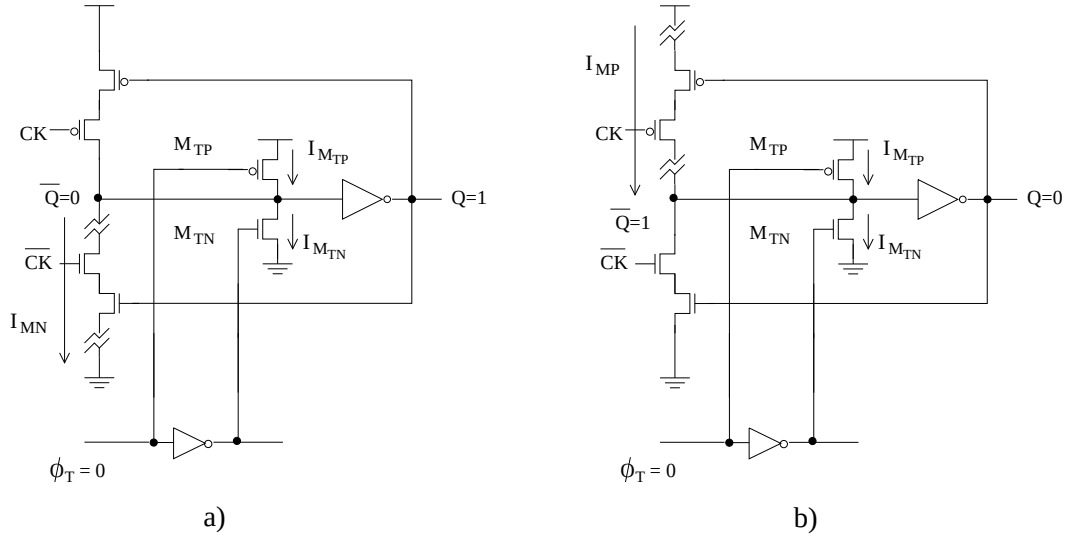


Figure 3.18: Topologies of the memorizing stage with the DFT circuitry for testing resistive opens in the Nmos network (incise a) and Pmos network (incise b) of the clocked inverter stage.

The behavior of the CMOS latch using the DFT circuitry is shown in Figure 3.19. Different resistance values for open R_{11} (See Figure 3.18) have been considered. The initialized state is given at the beginning of the Figure 3.19. During the activation phase (ϕ_T=0V), the voltage at the node Q ($\overline{Q}$) decreases (increases). The ϕ_T is disactivated. Resistive opens equal or higher than 30KΩ flip the state of the CMOS latch. Hence, these opens are detected. Resistive opens smaller than 30KΩ do no change the state of the latch. Hence, these opens are not detected.

The minimum detectable resistance value of the opens in the Nmos and Pmos

networks depends on the width of the activation signal (T_{WT}) and the channel ratio W_{MTP}/W_{MTN} of the two test transistors. The previous conditions must flip the state of the defective CMOS latch. At the same time, the fault-free CMOS latch must not change its state.

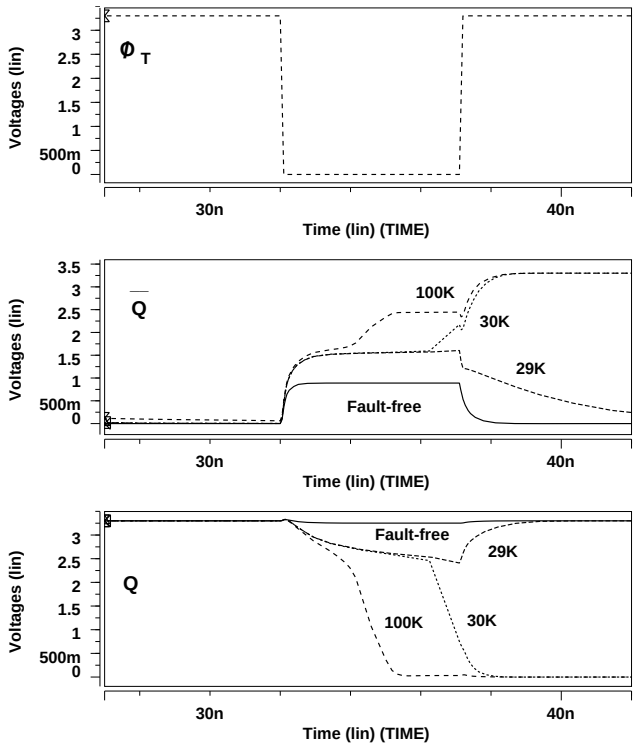


Figure 3.19: Timing diagram for DFT circuitry. Resistive open R_{11}, W_P=3μm, W_N=1.3μm, T_{WT}=5ns.

The required conditions to detect resistive opens in the CMOS latch are given in Figure 3.20. W_{MTP}/W_{MTN} is the required channel ratio of the two test transistors to detect a given resistive open. A proper W_{MTP}/W_{MTN} ratio must be chosen to be able to detect resistive opens in both Nmos and Pmos networks. The minimum detectable resistive open in the Nmos network (open R_{11} in Figure 3.20) decreases as the ratio W_{MTP}/W_{MTN} is made larger. The minimum detectable resistive open in the Pmos network (open R_8 in Figure 3.20) increases as the ratio W_{MTP}/W_{MTN} is made larger. The optimum W_{MTP}/W_{MTN} is the intersection of the curves (See Figure 3.20). At this point, the minimum detectable resistive open is optimized for both branches (Nmos and Pmos).

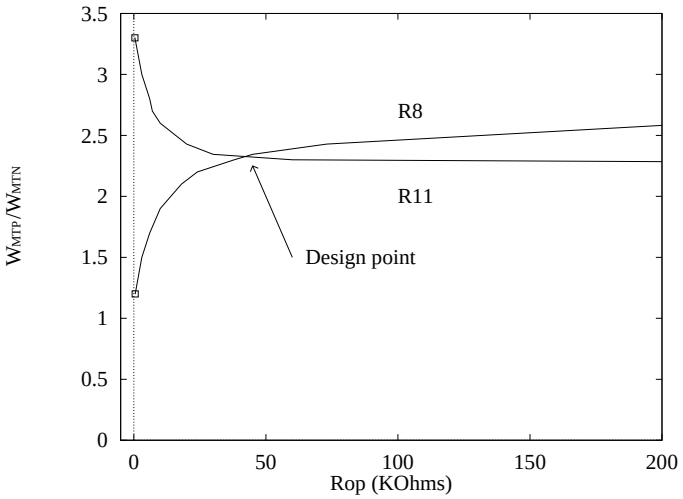


Figure 3.20: Channel width sizing of the DFT transistors M_{TP}, M_{TN}. Width activation signal T_{WT}=5.0 ns.

The cost of the proposed approach has been estimated in terms of speed degradation and area overhead (See Table 3.2). ΔT_d is the speed penalty (writing time) of the latch with the DFT transistors respect to the case without DFT circuitry. ΔA is the area penalty. R^{Det}_{Min}N (R^{Det}_{Min}P) is the value of the minimum detectable resistance of the open in the Nmos (Pmos) network. The actual value of W_{MTP}/W_{MTN} for R^{Det}_{Min} must be chosen taking into account the process corners. As can be seen in Table 3.2, the addition of the two DFT transistors do not degrade significantly the dynamic characteristics of the CMOS latch.

$\frac{W_p}{W_n}$	R^{Det}_{Min}N	R^{Det}_{Min}P	ΔT_d%	ΔA%
2.2	1MΩ	24KΩ	1.02 (4ps)	4.70
2.3	30KΩ	45KΩ	2.30 (9ps)	4.73
2.7	7KΩ	650KΩ	3.07 (12ps)	4.79

Table 3.2: Cost of the DFT. T_{WT}=5ns.

Table 3.3 shows a comparison between our proposals and other testable latch structures [80] [81]. Our first proposal proposal requires two additional inputs.

Our second requires only one additional input through the entire circuit and it can detect a parametric range of the open resistance. If routing is not considered, the second proposal consumes more area than the first one. Two signal proposal is more sensitive to detect resistive opens that one signal proposal. This is due to the fact there is not competition between the two DFT transistors, only one DFT transistor is activated while the other is disactivated.

Circuit	Add Trans.	Add Inputs	Number Vectors	R_{DET}
[80]	4	1	12	R_∞
[81]	4	2	8	R_∞
2 signal proposal	2	2	8	18K-∞
1 signal proposal	4	1	8	40K-∞

Table 3.3: Comparison with other testable latches.

At system level routing of only control signals is required. Hence, the impact of area of this approach is less than for the technique using two control signals. It is expected a minimal impact of the power consumption. At global circuit level, the additional input can be used for all the memory elements.

3.2.6 Summary of the Results

The most significative results for opens in the symmetrical latch are:

- For opens located in the driver stage the delay increases as the value of the resistive open increases. For a given resistive open there is a critical t^*_{xsu} which gives logic error in the latch. In other words, the timing relationship between the input data and the clock determines the logic behavior of the latch.

- High resistive opens located in the gates in the driver stage are influenced by initial conditions prior to the application of the two-vector sequence. For

detecting these opens, the latch output must be monitored for both vectors of the two-pattern sequence.

- High resistive opens in gates with intermediate voltages around $V_{DD}/2$ as initial conditions could be non detected by logic testing. Furthermore, these opens produce small delays. The cycle of the first vector should be long enough for detecting these opens or to have a writing time prior to the application of the two-pattern vector.

- Single open gates affecting the transistor driven by the clock signal in the driver inverter are also influenced by initial conditions. However, in these cases no anomalous behavior can be observed for the first vector of the two-pattern vector. Hence, only one vector can be applied to excite this open. Negligible delays appear for high voltages as initial conditions. High resistive opens affecting the transistor driven by the clock signal could be difficult to detect for certain initial conditions. A too long cycle time for the first vector should be required.

- Delays in the conductive paths are the higher observed. The smaller obtained delays correspond to opens affecting single gates.

- Opens located in the clocked inverter stage are in general hard to test. Most of them are undetectable by logic and delay testing. Care must be taken with opens in the feedback path. High resistive open in this location can produce a logic error under certain conditions. Opens in the control path remain undetectable. Layout techniques may be used to decrease the probability to occur of these opens.

- Two DFT proposals to test resistive opens in conducting paths of the clocked inverter stage have been proposed. Two control signal and one control signal proposals allow to detect these opens. Two signal proposal was more sensitive to detect resistive opens than one signal proposal. For both proposals the range of the detectable resistance was a function of the DFT width transistors and the activation pulse width.

- Resistive opens in the inverter stage have a similar behavior to that found for opens in the driver stage.

A summary of the possible exciting transitions for resistive opens in the symmetric latch is given in Table 3.4. The results are only given for opens in the Nmos networks. Opens located in a complementary position in the Pmos networks behaves similarly. The label DET^{ic} in Table 3.4 indicates that these opens are influenced by initial conditions. Hence, the exciting conditions for these opens should be properly applied. In other words the first vector should be applied for a sufficiently long time for having initial conditions which produce significant delays.

Stage	Open	Testability	Vectors
DS	R_{10}	DET	0→1
	R_4	DET	0→1
	R_{13}	DET^{ic}	0→1 & 1→0
	R_{17}	DET^{ic}	0→1
	R_{22}	DET^{ic}	0→1 & 1→0
CIS	R_6	DET	1→0
	R_{12}	DET	1→0
	R_{19}	DET^{ic}	0→1 & 1→0
	R_{27}	DET^{ic}	0→1 & 1→0
OS	R_5	Non DET	—
	R_{11}	Non DET	—
	R_{18}	Non DET	—
	R_{21}	Partial DET	0→1

Table 3.4: Testability of Resistive Opens in the Symmetric CMOS latch cell. DS: Driver Stage. OS: Output Stage. CIS: Clocked Inverter Stage.

Opens	Output Behavior
Conducting Paths (DS and OS)	delay, logic error
Open Gates (DS and OS)	delay, logic error (ic)
Conducting Paths (CIS)	data retention fault
Control Path (CIS)	data retention fault
Feedback Path (CIS)	data retention fault, logic error (ic)

Table 3.5: Summary Behavior of the Symmetric CMOS Latch. (ic) initial condition dependent. DS: Driver stage, OS: Output stage, CIS: Clocked inverter stage.

In Table 3.5, the output behavior of resistive opens is summarized. Resistive opens in conducting paths affecting the driver and output stages can be mapped to the output of the CMOS latch as delay fault or logic error. These opens are dependent on the timing relationship between the data and the clock signal. Resistive opens in gates affecting the driver and output stages are also timing dependent. In addition, the initial condition influences the detectability of these opens. These opens can be mapped to the output of the CMOS latch as delay fault or logic error. Sufficiently high resistive opens in the clocked inverter produces a data retention fault. It must be noted that low values of resistive opens do not produce a data retention fault because a low impedance path to V_{DD} (GND) is created. Some opens in the feedback path can also be mapped to the output of the CMOS latch as a logic error or data retention fault depending on the resistance value of the open and the initial voltage condition.

3.3 Analysis in the transmission gate CMOS latch

In this section the behavior of a transmission gate (TG) CMOS latch cell under resistive opens is investigated. A two-vector test input is also applied. Parameter t_{xsu} is the same that used for the symmetrical CMOS D-latch cell.

3.3.1 Transmission gate CMOS latch

The schematic of a TG CMOS latch cell is shown in Figure 3.21. This CMOS latch is composed by the following stages: input stage, inverter stage and closing memory stage.

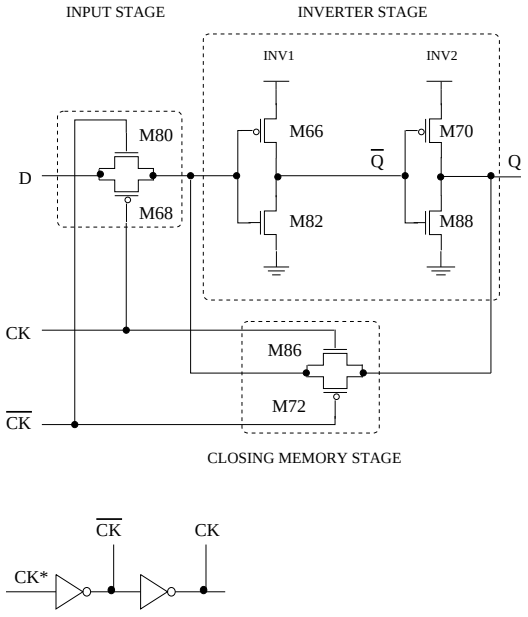


Figure 3.21: Schematic diagram of the TG CMOS latch cell.

The analyzed resistive opens in the TG latch are shown in Figure 3.22. Resistive opens are considered in all the vias and contacts. Resistive opens have been considered as lumped resistances with a continuous range of values. Only those cases affecting the Nmos network are analyzed. Cases in the Pmos network can be analyzed in a similar way.

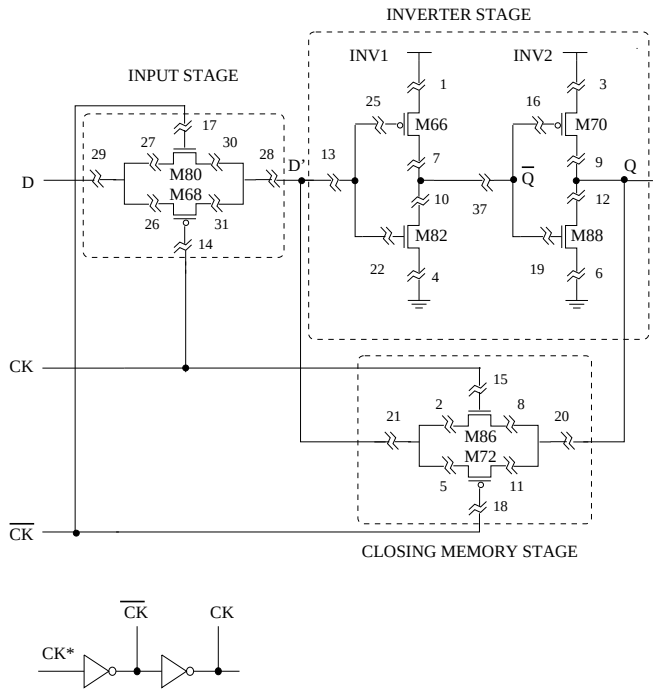


Figure 3.22: Analyzed resistive open in the TG CMOS latch cell.

It is analyzed the testability of the TG latch by logic and delay testing. A two-test vector sequence is used. A first vector initialize the latch, then a second vector try to toggle the state of the latch. The parameter t_{xsu} is also used to analyze the testability of the latch. The analysis has been made for resistive opens located in each stage of the latch. Resistive opens in the conducting paths and resistive opens in gates are analyzed. Opens in gates include those affecting to one gate or multiple gates.

3.3.2 Resistive opens in the input stage

Two cases are found: a) when the open affects both transistors (See Figure 3.22) of the TG, and b) when the open affects one transistor (See Figure 3.22) of the TG. The opens have been classified as follows:

- Conducting path: R_{29}, R_{27}, R_{30}, R_{28}, (R_{26}, R_{31})
- Single open gates: R_{17}, (R_{14})

Resistive opens in conducting paths

First, it is analyzed the case when both transistors (R_{29}, R_{28}) of the transmission gate are affected (See Figure 3.22). Then the case of one affected transistor (R_{27}, R_{30}) of the transmission gate is analyzed.

- Resistive opens affecting both transistors of the TG

This open affects the current trajectory in both transistors of the TG. The time to charge node D' (See Figure 3.22) is a function of the capacitance in node D' and the equivalent resistance of the TG plus the resistive open. As a consequence, the delay increases. The expected delay for this class of resistive open is the highest for opens in conducting path.

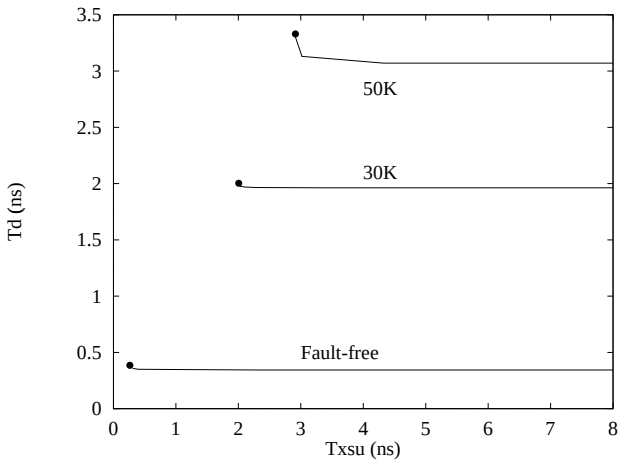


Figure 3.23: t_{delay} for moderate resistive open R_{29}.

The obtained delay as function of t_{xsu} for resistive open R_{29} (See Figure 3.22) is shown in Figure 3.23. A larger delay is obtained as the value of the R_{open} increases. For a certain low value of t_{xsu} the TG latch will not operate logically correctly. This condition is indicated with a dot in Figure 3.23.

High resistive opens are also affected by initial voltage conditions. Intermediate voltage conditions at the gate of the Nmos and Pmos transistors of the inverter INV1 can produce partially conduction of both defective transistors. The final

state of the latch is influenced by the value of the initial conditions. Large delays can appear. The delay time for a resistive open of 1MΩ for both input data transitions is shown in Figure 3.24.

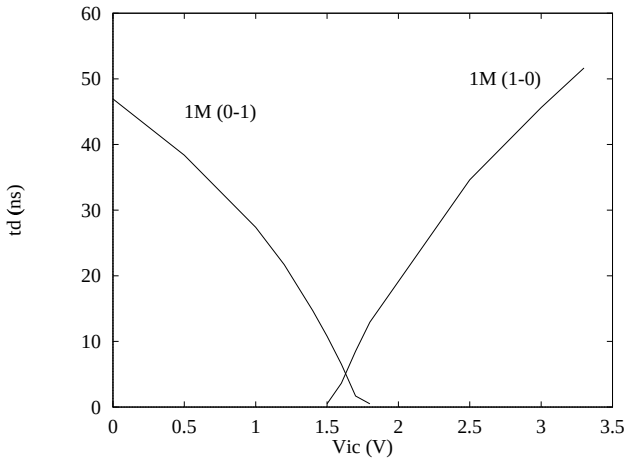


Figure 3.24: t_{delay} for high resistive open R_{29}.

For 0→1 transition and low initial voltage conditions, large delays are observed because the initial voltage condition favours turning-on the Pmos transistor M66 (See Figure 3.22). The node at the right of the resistive open is slowly charged according to the input data. The delay decreases as the initial voltage condition increases. A similar behavior can be observed for the 1→0 transition. Resistive opens with intermediate initial conditions produce small delays for both input transitions. Opens with these conditions are more difficult to detect by delay testing.

- Resistive opens affecting only one transistor of the TG

The resistive opens considered in this case are R_{27} and R_{30} (See Figure 3.22). These opens affect the conducting path of the Nmos transistor of the TG. Small delay increments are expected for these opens because only the current trajectory through the Nmos transistor is affected. The current trajectory through the Pmos transistor remains fault-free. Because there is a non-affected current trajectory the delays will not increase significantly. This is shown in Figure 3.25. Data D and clock CK signals are shown in the upper panel. Data transition takes place in writing (clock low) phase. Output node Q is shown in lower panel for fault-free,

10KΩ, 50KΩ and 1MΩ cases. It can be observed that the delay is small even for high resistive opens. The delay time as function of t_{xsu} is shown in Figure 3.26. These opens are difficult to detect by delay testing or logic testing because the low values of t_d and t^*_{xsu}.

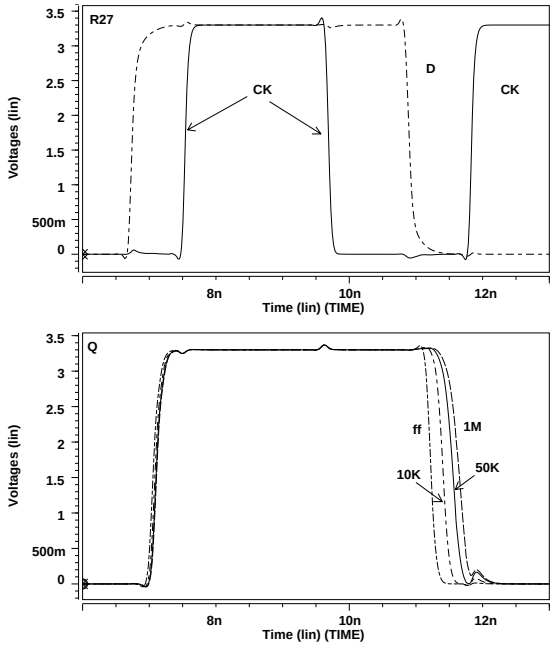


Figure 3.25: Timing diagram of resistive open R_{27}.

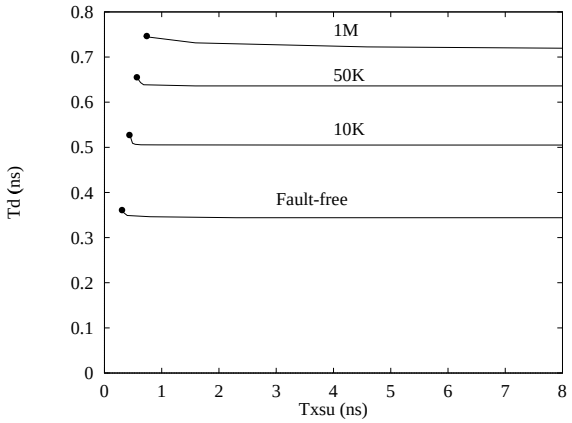


Figure 3.26: t_{delay} for resistive open R_{27}.

Single open gates

The resistive open analyzed in this case is R_{17} which is located at the gate of Nmos transistor of the transmission input gate. The impact of this open is not severe because the Pmos transistor M68 (See Figure 3.22) is not affected. This is similar to the case when the open affect one transistor of the input TG. The worst scenery is for the condition of the Nmos transistor M80 cut-off and the Pmos transistor M68 turned-on (See Figure 3.22). Under these conditions the input data goes only through Pmos transistor. The total input resistance is the drain-source Pmos transistor. The non-affected transistor assures a fault-free conducting path. As a consequence the delays are small.

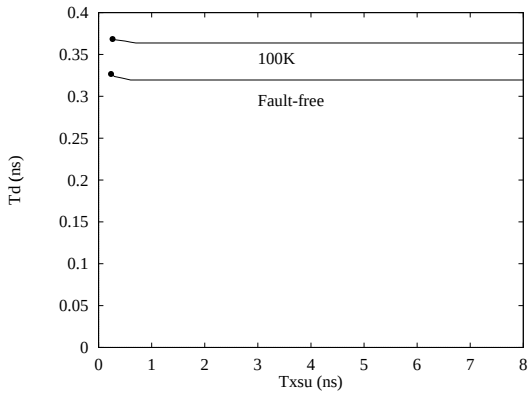


Figure 3.27: t_{delay} for resistive open R_{17}.

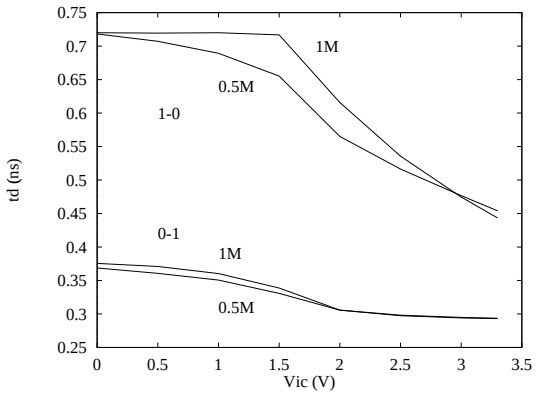


Figure 3.28: t_{delay} for high resistive open R_{17}.

Time delay t_d as function of time t_{xsu} for different moderate resistive R_{open} is shown in Figure 3.27. The delay increment is small. This open is difficult to detect by delay or logic testing. The behavior is similar for the condition of high resistive opens. The delay for transition 0→1 and 1→0 are shown in Figure 3.28. Low initial voltage conditions produce the most severe delay because the Nmos faulty transistor is disabled. These opens are difficult to detect because the small obtained delays.

3.3.3 Resistive opens in the inverter stage

The opens in this stage can be analyzed considering separately each inverter (See Figure 3.22):

a) Opens affecting inverter INV1

b) Opens affecting inverter INV2

- Opens affecting INV1

The behavior of these opens is similar to that found for the driver inverter and output stages of the symmetrical CMOS latch. In this case there are not clock signals. In a general form, the opens in this stage are divided into resistive opens in the conducting path and resistive opens in the gates. Opens in the conductive path can be detected by delay testing or logic testing. They are timing depending on the clock and data signals. One input data transition is applied to test them. Open in gates are harder to detect that opens in the conductive path. Faults in gates are depending on the initial conditions. Large delays can be obtained when the first vector is applied for sufficient long time. Initial conditions around $V_{DD}/2$ produce small delays. These resistive opens are more difficult to detect.

- Opens affecting INV2

Opens affecting INV2 (See Figure 3.22), except multiple open gate R_{37}, are influenced by charge sharing. Reddy et al. [80] and Al-Assadi et al. [79] have also observed charge sharing in the transmission gate latch for stuck-open faults. Charge sharing can occur for resistive opens in the conducting paths or in a single gate. The first vector of the sequence of two vectors can be invalidated. When the first vector is invalidated the open is not detected. Charge sharing takes place between nodes Q and D' (See Figure 3.29). The stored charge in nodes Q and D' is shared when the TG in the feedback loop is activated. The final state of the latch is determined by the voltages at nodes Q and $\overline{Q}$ after charge sharing and the input/output transfer characteristics of the inverters in the feedback loop [89]

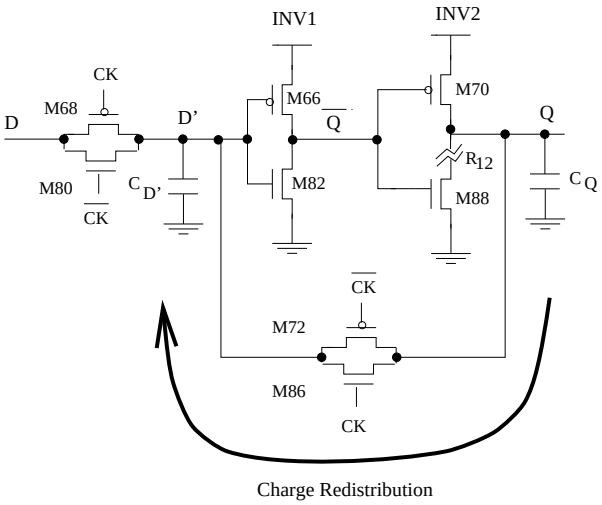


Figure 3.29: Charge sharing effect.

[83] [97].

Let's analyze resistive open R_{12} (See Figure 3.29). A high logic value at node Q is stored for the first vector. During the writing phase of the second vector a low logic at the input data tries to discharge node Q. However, node Q does not completely discharge due to the resistive open. Note that node D' has a well defined low logic level. When the memory phase of the second vector begins, the transmission gate in the feedback loop closes (See Figure 3.29). As a consequence the charge is redistributed between nodes Q and D'. The test pattern is invalidated if the voltage at node Q after charge sharing makes the defective latch to switch according to the input data of the second vector. In other words, the vector is invalidated if the voltage at node Q (See Figure 3.29) switch to a low logic level.

The simulation results for resistive open R_{12} are shown in Figure 3.30. The value of the resistive open is 180KΩ. Clock CK and data D signals are shown in the upper panel (See Figure 3.30). Data changes in writing phase. The output Q of the latch is given in the lower panel. Charge sharing takes place when the memory phase begins. Curve D2 shows the case where charge sharing helps to the flip-flop to reach the correct logic state. In this case the test vector is invalidated. For curve D0 charge sharing is not enough to reach the correct logic state. Logic

error is generated and the defect can be detected by logic testing.

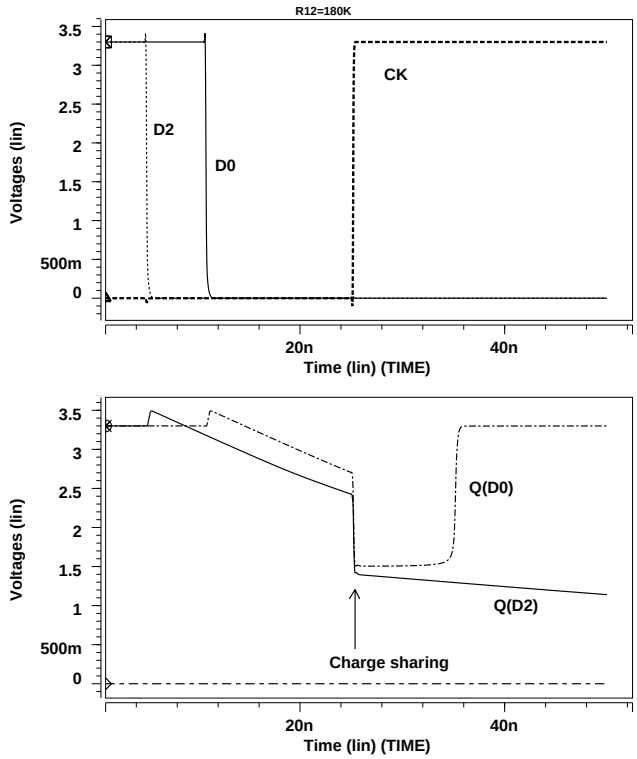


Figure 3.30: Charge sharing effect for fault R_{12} (180KΩ). Upper panel.- clock CK, data D. Lower panel.- Node Q. D0.- t_{xsu}= 14.39ns. D2.- t_{xsu}= 20.19ns.

Under charge sharing and high resistive opens the output node takes a longer time to reach well defined logic values. The measured delays for moderate resistance values for open R_{12} are shown in Figure 3.31. Delay increases as t_{xsu} is close to its critical value. Moderate resistive opens produce high delays. It must be noted that time delay t_d, in the analyzed cases, has been measured from 90% to 10% of V_{DD}.

The impact of charge sharing in the latch behavior can also be seen as a decrement on the time t^*_{xsu}. Figure 3.32 illustrates this effect. Cases for charge sharing (cs) and no charge sharing (no_cs) are taken into account. The behavior of charge sharing and no-charge sharing cases can be divided in two parts: a) the first part for low resistive opens, and b) the second part for moderate and high resistive

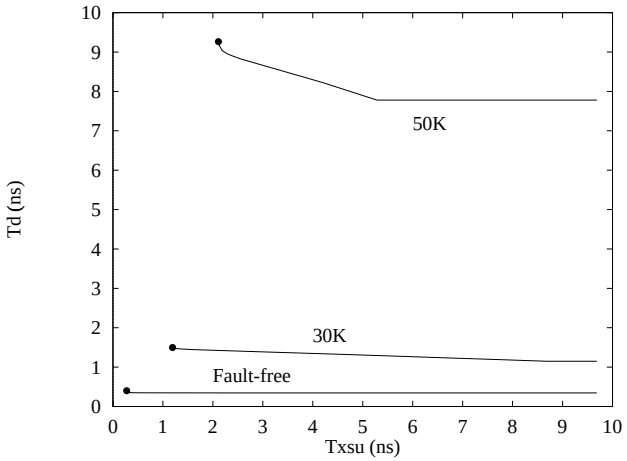


Figure 3.31: t_{delay} for resistive open R_{12}.

opens. For low resistive opens, the curve without charge sharing has lower t^*_{xsu} than the charge sharing curve. This is because charge sharing has low impact for low resistive opens. For high resistive values, transistor M88 (See Figure 3.29) conducts weakly. Charge is transferred from node D' to node Q. This charge is not drained sufficiently fast through transistor M88. Charge sharing curve (cs) requires a smaller t^*_{xsu} time than the non-charge sharing curve (no_cs). A smaller value of t^*_{xsu} makes the open more difficult to detect.

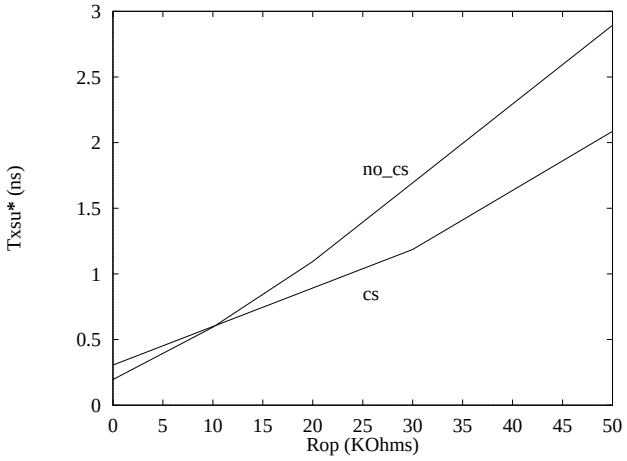


Figure 3.32: t^*_{xsu} for resistive open R_{12}. Non-charge sharing case (no_cs). Charge sharing case (cs).

A first order analytical expression considering charge sharing effect has been developed. Resistive open R_{12} is considered. The analysis is divided in two parts. The first part takes into account the writing phase of the second vector (D=0) and the partial discharge of node Q. The second part considers the memorizing phase of the second vector, when charge sharing between nodes D' and Q takes place.
The first part that defines the discharge of node Q can be expressed by:

$$V_Q^{bcs} = V_{DD} e^{-t_w / RC_Q} \tag{3.1}$$

where V_Q^{bcs} is the voltage at node Q (See Figure 3.29) before charge sharing, V_{DD} is the voltage of the power supply, t_w is the writing time of the second vector, C_Q is the capacitance related to node Q, R is the resistance of the open plus the drain-source resistance of the affected transistor.

Neglecting the resistance of the TG and conduction through the defective transistor, the voltage at node Q after charge sharing (V_Q^{acs}) can be estimated by:

$$V_Q^{acs} = \frac{C_Q V_Q^{bcs}}{C_Q + C_{D'}} + \frac{C_{D'} V_{D'}}{C_{D'} + C_Q} \tag{3.2}$$

where $V_{D'} = 0$, $C_{D'}$ is the capacitance related at node D'.

After substituting equation 3.1 in 3.2 the following expression is obtained:

$$V_Q^{acs} = \frac{C_Q}{C_Q + C_{D'}} V_{DD} e^{-t_w / RC_Q} \tag{3.3}$$

It must be noted that a voltage V_Q^{acs} produces a corresponding voltage $\overline{V_Q^{acs}}$ for the other inverter in the memory circuitry (See Figure 3.29). The output latch will evolve to 1 or 0 logic depending on the voltage V_Q^{acs} and the input/output transfer characteristics of the two inverters in the memory circuitry.

The capacitances C_Q and $C_{D'}$ have close values in the analyzed latch structure (See Figure 3.29). There is an equal number of transistors and diffusion capacitances connected to each node Q and D'. The output node Q has one inverter as load (not shown in Figure 3.29).

In equation 3.3, the different parameters influencing charge sharing are observed. The right term represents the discharge of node Q during the writing phase of the second vector. The left term considers charge sharing once the feedback loop is closed. For the second vector, the final V_Q^{acs} is low for large writing times or low resistive opens. In this case the open is not detected. For very high resistive opens the voltage at node Q has a high logic value at the end of the writing phase of the second vector. Intermediate voltages at node Q, before charge sharing, can appear for not very large writing times or higher values of resistive opens. Assuming equal values for C_Q and $C_{D'}$, because charge sharing the voltage at node Q decreases at half the value before charge sharing as can be seen in the left term of equation 3.3. This is true as long as the resistive open is sufficiently high for neglecting the current path through the defective transistor. It can be concluded that charge sharing helps to invalidate the test vector.

3.3.4 Resistive opens in the closing memory stage

Resistive opens in the closing memory stage (See Figure 3.22) have been classified as follows:

- Opens in control path: R_{15} (R_{18})
- Opens in conducting paths: R_{20}, R_8, R_2, R_{21} (R_{11}, R_5)

Resistive opens in conducting paths

Opens located in this position are not detectable by logic or delay testing. Opens affecting only one transistor of the TG such as R_2, R_8, R_5, R_{11} (See Figure 3.22) do not degrade the logic level of the transmission gate. These opens remain undetectable. Layout techniques should be used to reduce the probability to occur of these opens [95]. In addition very high resistive opens affecting

both transistors of the TG may suffer a data retention fault. A DFT approach is proposed for these opens in the next subsection.

Resistive opens in the control path

Resistive open R_{15} is analyzed (See Figure 3.22). High resistive opens in the control path of closing memory stage may produce a delay increment. But the delay increment is small.
When there is a high (low) voltage as initial condition at the gate of Nmos M86 (Pmos M72) at the beginning of the writing phase, the transistor M86 (M72) does not turn-off (See Figure 3.33). Nodes Q and D' remain connected (See Figure 3.33). Let's apply the 1→0 input data transition. When the input D changes to "0" then a competition between the Pmos transistor of the input inverter and the Nmos transistor of INV2 takes place because M86 (M72) is on (See Figure 3.33). The winner of the competition is the Pmos transistor.

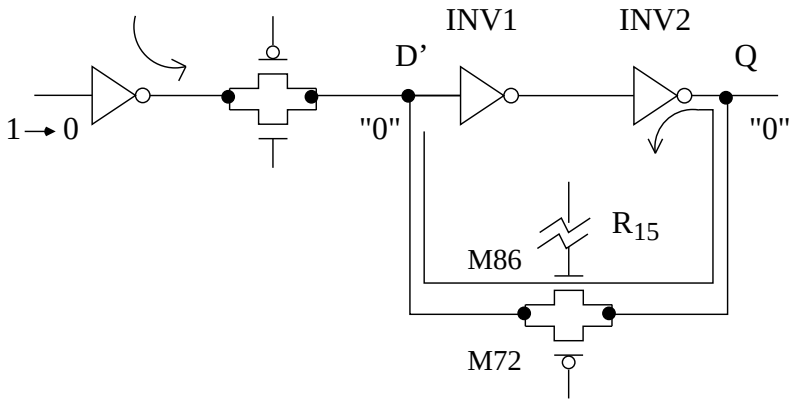


Figure 3.33: Networks competence due to R_{15}.

Figure 3.34 shows the additional delay obtained. Figure 3.35 shows the delay for high resistive opens as function of initial voltage conditions. The delay increment for the 1→0 transition. Resistive open R_{15} is hard to be detected by delay testing or logic testing.

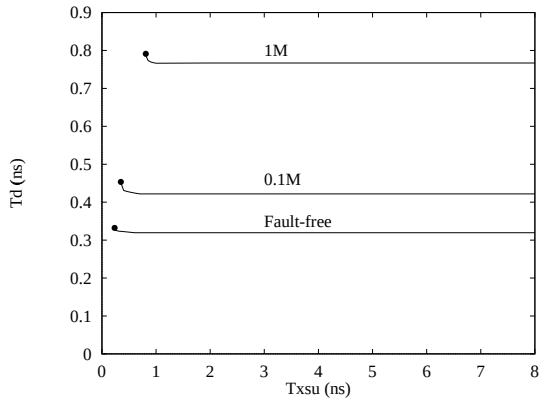


Figure 3.34: t_{delay} for high resistive open R_{15}.

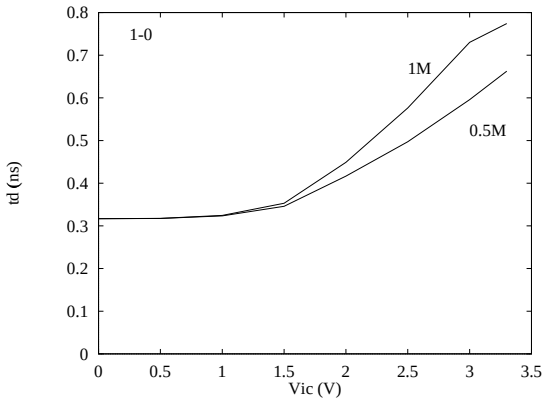


Figure 3.35: t_{delay} for resistive open R_{15}. 1MΩ curve with initial condition voltage V_{ic}=3.3V.

3.3.5 A DFT testable latch cell

In this subsection a DFT circuitry to test resistive opens in the conducting path of the closing memory stage is proposed. The proposed circuitry is shown in Figure 3.36.

An Nmos transistor has been added to node D'. The resistive opens in the conducting path are tested as follow:

- Initialize the latch to 1 logic.
- In memory phase, activate the Nmos DFT transistor.
- Disactivate the Nmos DFT transistor.
- Observe the output of the CMOS latch.

Let's consider resistive open R_{21} (See Figure 3.36). The initialized state is given at the beginning of the Figure 3.37. During the activation phase (ϕ_{TN}=1), the voltage at the node Q ($\overline{Q}$) decreases (increases). Resistive opens equal or higher than 4.3KΩ flip the state of the TG CMOS latch. Hence, these opens are detected. Resistive opens lower than 4.3KΩ do no change the state of the latch. Hence, these opens are not detected.
The minimum detectable resistance value of the open is determined by the width

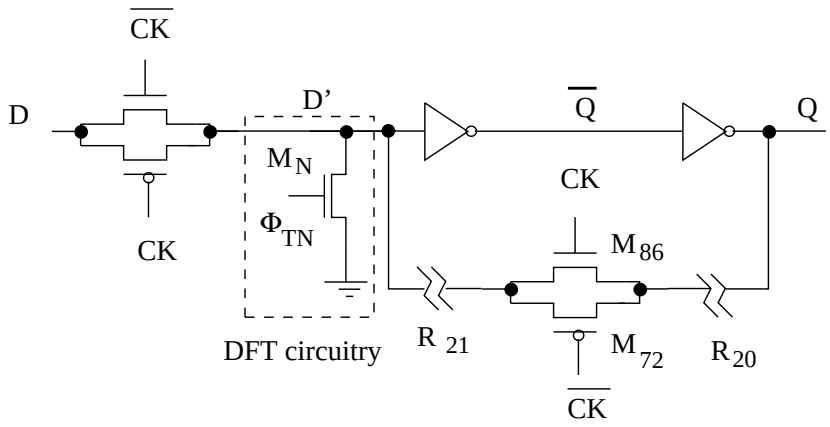


Figure 3.36: Proposed DFT circuitry used to detect resistive opens in the clocked feedback stage.

of the activation signal (ϕ_{TN}) and the channel width of the DFT Nmos transistor M_N. The previous conditions are chosen to flip the state of the defective TG CMOS latch. At the same time, the fault-free CMOS latch must not change its state.

Figure 3.38 gives the conditions of ϕ_{TN} and W_n necessary to detect the resistive open R_{21}. T_{wt} is the width of activation pulse and W_n^* is the minimum width of the DFT transistor. The width of the DFT transistor W_n^* decreases as the width of activation pulse T_{wt} increases. Small resistive opens can be detected if the width of W_n or T_{wt} are increased.

Resistive opens affecting both drain or source of transmission gate such as R_{21} or R_{20} (See Figure 3.22) can be easily detected that those cases affecting only one transistor. This is because the fault-free transistor assures a low impedance in the conducting path. In Figure 3.39, the minimum width of the DFT transistor used to detect resistive open R_2 is shown. Small variations in the W_n^* indicates that these cases can be difficult to detect with the DFT circuitry. Smaller widths of the DFT transistor W_n is required in this case to those cases affecting both transistors of the TG. Resistive opens affecting to only one drain or source are difficult to detect because small variations in the width of DFT transistor can be interpreted as defective.

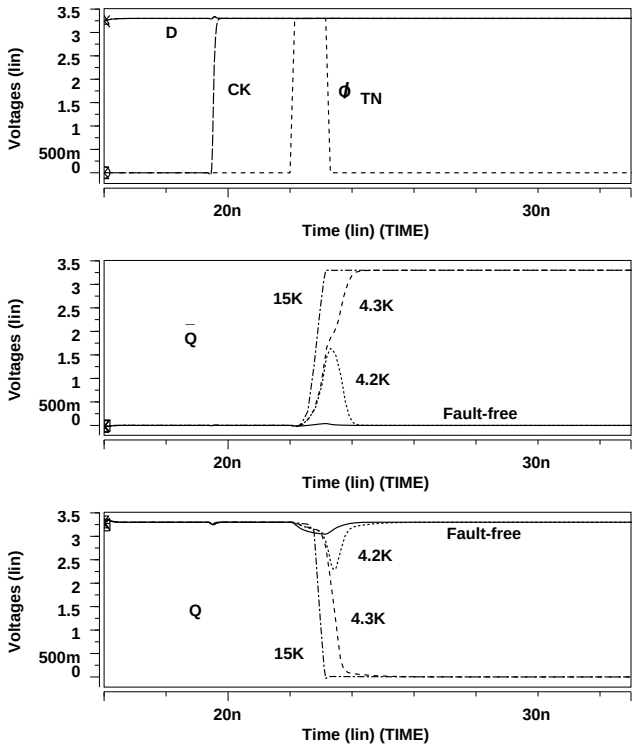


Figure 3.37: Timing diagram for resistive open R_{21}, W_n= 0.6μm.

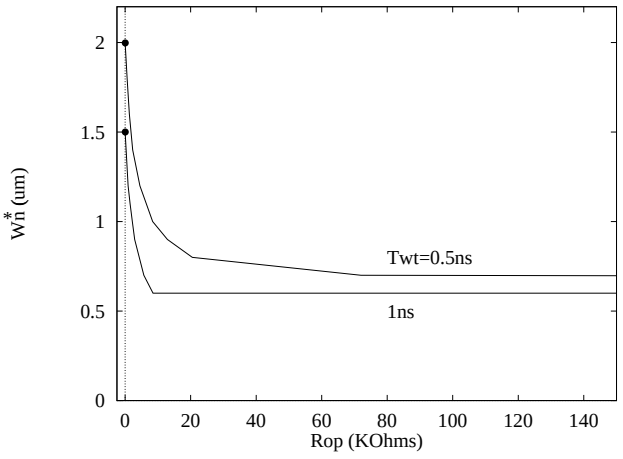


Figure 3.38: Minimum width W_n needed to detect resistive open R_{21}

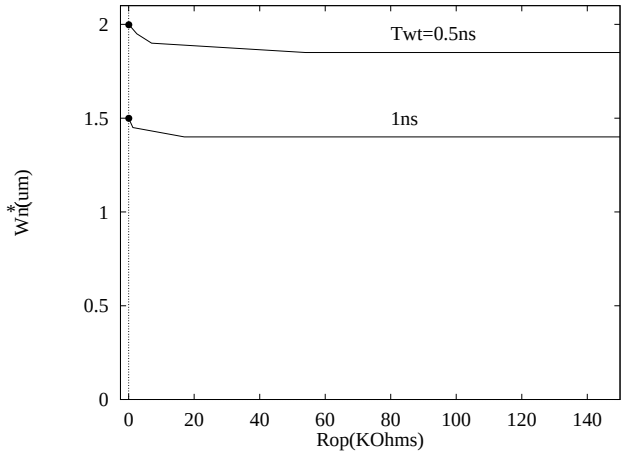


Figure 3.39: Minimum width W_n needed to detect resistive open R_2

3.3.6 Summary of the results

The most significative results for opens in the TG latch are:

- The delay increases for opens affecting both transistors of the TG in the input stage. For a given t_{xsu}, the delay increases as the resistive open increases. For a given R_{op} there is a critical t^*_{xsu} producing logic error in the TG latch. High resistive opens are influenced by initial conditions.

- The delay just slightly increases for opens located in conducting paths affecting one transistor of the input stage. Because the open affects only one transistor of the TG, the complementary transistor remains fault-free and represents a fault-free current path. These opens are hard to detect.

- Opens in inverter INV1 of the inverter stage behaves similarly to opens located in the driver and output inverter of the symmetric CMOS latch. Conditions to test them are also similar.

- Opens located in inverter INV2 of the inverter stage, except multiple opens gate, are affected by charge sharing. The impact of this effect is that the second vector can be invalidated and the defect is not detected. The critical t^*_{xsu} for producing a logic error decreases. For single open gates moderate values of resistive opens produce low values of critical t^*_{xsu}. A low critical

t^*_{xsu} value will make more difficult to discriminate a defective behavior from the fault-free behavior.

- Resistive opens in conducting paths of the closing memory stage are not detectable by logic or delay testing. Open defects affecting both transistors of the TG are similar to those found in conducting paths of the clocked inverter in the symmetric CMOS latch. These defect may suffer a data retention fault. Open defects affecting one transistor of the TG do not produce a data retention fault.

- High resistive opens in the control path of the closing memory stage increases the delay for certain initial conditions. Even so these defects are hard to detect.

- Some opens in the conducting path of the closing memory stage can be detected if a DFT circuitry is added.

A summary of the possible exciting conditions for resistive opens in the TG latch is given in Table 3.6. Only results for the Nmos network are given. Similar results for the Pmos network can be obtained. DET^{cs} indicates that these opens are influenced by charge sharing. DET^{ic} indicates that these opens are influenced by initial conditions.

The output behavior of the resistive opens in the TG latch is summarized in Table 3.7. Resistive opens at the input stage can be observed as delay increment or logic error at the output. However, opens affecting only one transistor of the TG are difficult to detect. Resistive opens in gates affecting the input stage can be mapped at the output of the CMOS latch as delay or logic error. Conducting path opens in the closing memory stage are not detectable by either logic or delay testing. Opens affecting both transistors of the TG in the conducting path of the closing memory stage may produce a data retention fault. Opens in the control path of the closing memory stage could be detected by delay or logic testing. However, these opens are difficult to detect. Resistive opens in the output stage can be observed as a delay increment or logic error at the output. Those opens are influenced by charge sharing effects.

Stage	*Open*	*Testability*	*Vectors*
IS	R_{29}	DET^{ic}	0→1 & 1→0
	R_{28}	DET^{ic}	0→1 & 1→0
	R_{27}	Hard DET	0→1 & 1→0
	R_{30}	Hard DET	0→1 & 1→0
	R_{17}	Hard DET	0→1 & 1→0
INVS	R_{13}	DET^{ic}	0→1 & 1→0
	R_{37}	DET^{ic}	0→1 & 1→0
	R_{19}	DET^{cs}	0→1 & 1→0
	R_{22}	DET^{ic}	0→1 & 1→0
	R_4	DET	0→1
	R_{12}	DET^{cs}	1→0
	R_{10}	DET	0→1
	R_6	DET^{cs}	1→0
CMS	R_{20}	Non DET	—
	R_{21}	Non DET	—
	R_2*	Non DET	—
	R_8*	Non DET	—
	R_{15}	Hard DET	0→1

Table 3.6: Summary of the behavior of CMOS transmission gate latch. * hard to be detected. *ic*: initial condition dependency. *cs*: charge sharing dependency. IS: Input Stage. INVS: Inverter Stage. CMS: Closing Memory Stage.

Opens	Output Behavior
Conducting Path[1] (IS)	small delay
Conducting Path[2] (IS)	delay or logic error (ic)
Open Gates (IS)	delay (ic)
Control Path (CMS)	delay or logic error
Conducting Path[1] (CMS)	no error
Conducting Path[2] (CMS)	data retention fault
Conducting Path (INV1 of INVS)	delay or logic error
Open Gates (INV1 of INVS)	delay or logic error (ic)
Conducting Path (INV2 of INVS)	delay or logic error (cs)
Open Gates (INV2 of INVS)	delay or logic error (ic, cs)

Table 3.7: Summary Behavior of the Transmission Gates CMOS Latch. (ic) initial condition dependent. (cs) charge sharing dependent. IS: Input stage, CMS: Closing memory stage, INVS: Inverter Stage, Conducting Path[1]: affected one transistor of the TG, Conducting Path[2]: affected both transistor of the TG.

3.4 Analysis in the symmetric flip-flop cell

In this section, the behavior of opens in the latches is extended to a symmetric flip-flop structure. This analysis focused mainly how the defects violate the t_{xsu} of the affected latch of the flip-flop. Additionally, a defect in the master latch of the flip-flop may violate the timing conditions of the slave latch. This is considered in the context of the scan-path chain analyzed in section 3.6. The influence of charge sharing in the testability of some opens is analyzed.

3.4.1 General topology

In this subsection, the behavior of a symmetric flip-flop cell in the presence of resistive opens is analyzed. A block diagram of the flip-flop is shown in Figure 3.40. The master latch receives the input data D and its output Q_{LM} is the input of the slave latch. The output of the slave latch Q defines the output of the flip-flop.

The block diagram of Figure 3.40 can be represented at transistor level as

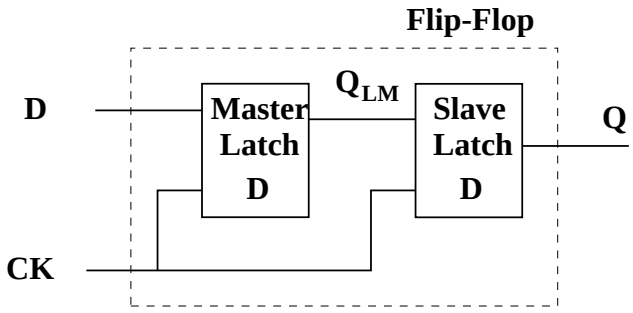


Figure 3.40: Block diagram of CMOS flip-flop.

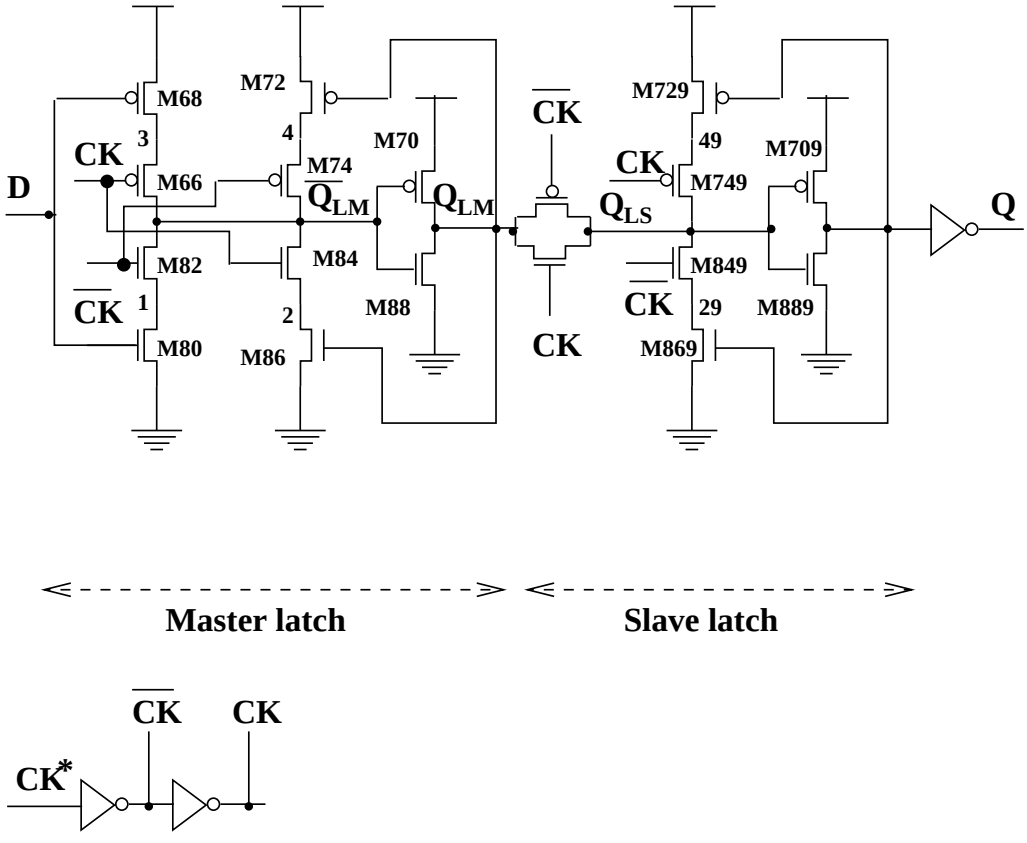


Figure 3.41: Symmetric CMOS flip-flop diagram.

shown in Figure 3.41. This flip-flop is activated by the positive clock transition. The schematic of the analyzed symmetric CMOS flip-flop with all the considered resistive opens is shown in Figure 3.42.

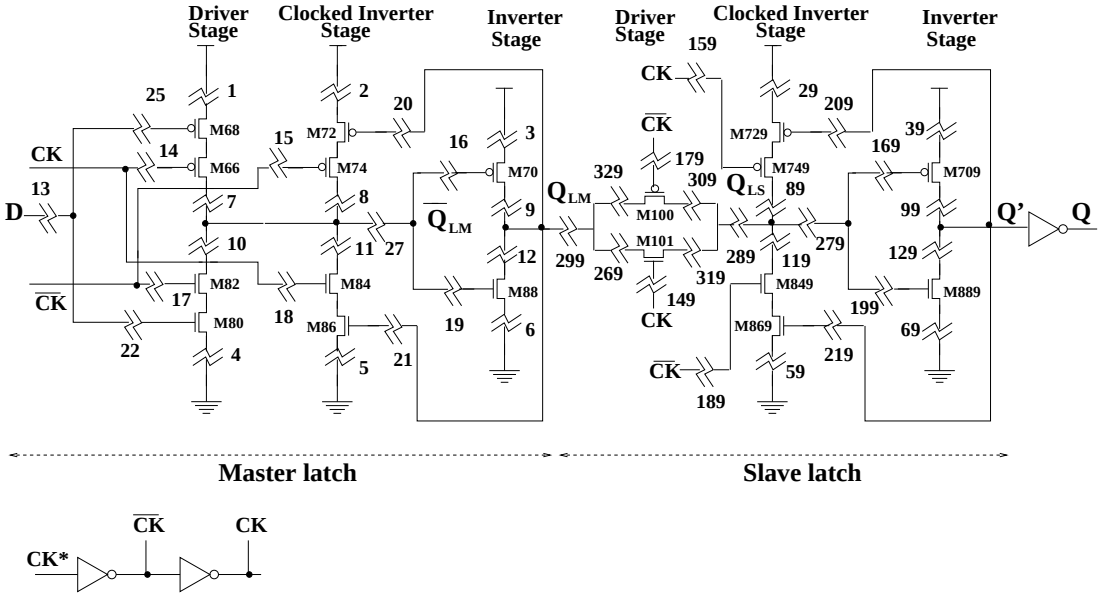


Figure 3.42: Resistive opens in the symmetric CMOS flip-flop.

The analysis of the symmetric CMOS flip-flop has been divided in:

a) Analysis in the master latch

b) Analysis in the slave latch

Resistive opens in master latch are analyzed with the parameter t^*_{xsu}. Time t^*_{xsu} is the critical t_{xsu} for a logic error to occur at the defective latch of the flip-flop. Opens in the slave latch are analyzed with the parameter t^*_{xsu}. Delay testing conditions are also investigated.

3.4.2 Analysis in the master latch

A resistive open in the master latch can produce additional delay at the output of the master latch. This additional delay could violate the timing conditions of the fault-free slave latch and a logic error to appear at the output of the flip-flop. This is analyzed in the context of a scan-path chain as previously stated. Besides, a logic error can also appear at the master latch output when the timing conditions, for a given resistive open, between the input data and clock are violated. The timing conditions have been defined using the variable t^*_{xsu}. A logic error at the master latch output is then transmitted to the output of the flip-flop.

Taking into account the stages of the master latch, it can be stated:

- The behavior and the detectability conditions for resistive opens located in the driver and clocked stages of the master latch are similar to those found in the same stages in the symmetric CMOS latch.
- In addition, resistive opens located at the output inverter of the master latch are influenced by charge sharing.

Opens in the driver and clocked stages of the master latch

Most opens located in the clocked stage are undetectable by logic or delay testing. Only very high resistive opens located in the control path (R_{20}, R_{21} in Figure 3.42) could give a logic error.
Opens in the driver stage can produce logic error when the timing condition t^*_{xsu} is violated. Resistive open R_{10} (See Figure 3.42) is considered to illustrate this behavior. This open is located in the Nmos network in the driver stage of the master latch (See Figure 3.42). A two test vector is used to excite this open. A first vector T1 (D=0) initialize the flip-flop to low logic value. Then, a second vector T2 (D=1) is applied (See Figure 3.43). For a fault-free behavior, the output Q of the CMOS flip-flop writes and memorizes correctly the input data D. However, a logic error for moderate resistive opens (See Figure 3.43) appears. A logic error appears for resistive opens higher than 30KΩ (See Figure 3.43).

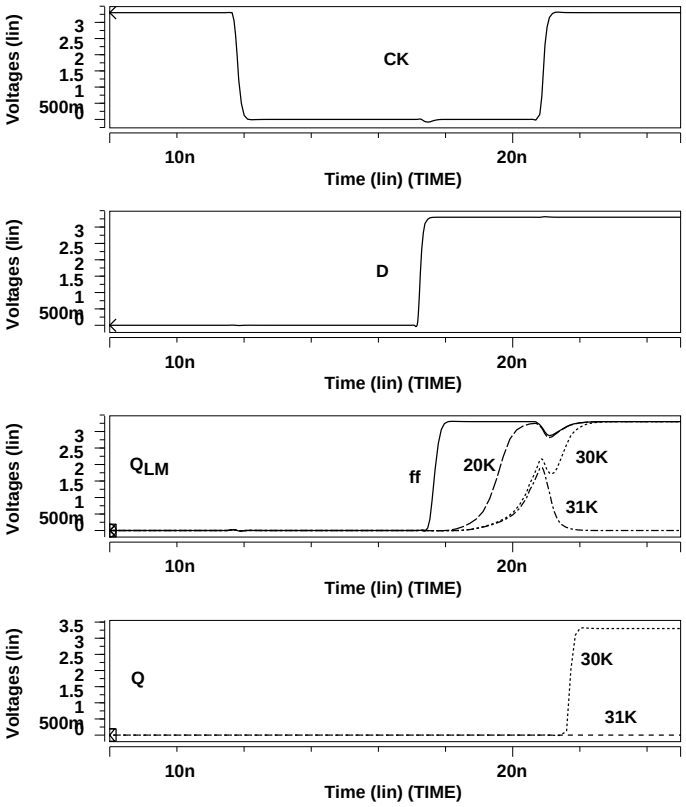


Figure 3.43: Timing diagram for resistive open R_{10}.

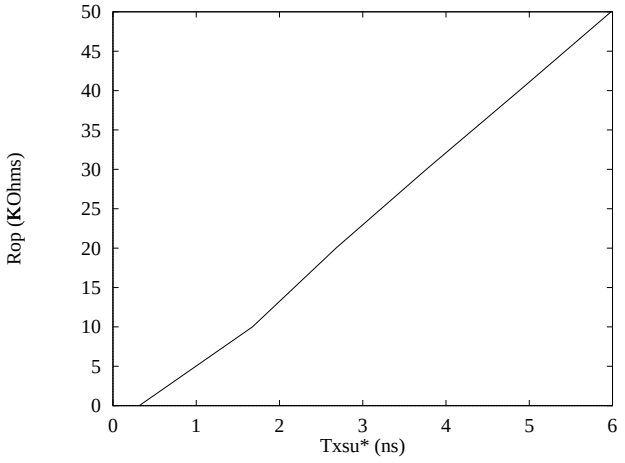


Figure 3.44: t^*_{xsu} for moderate resistive open R_{10}.

The required t^*_{xsu} for detecting a given open resistance is given in Figure 3.44. A higher t^*_{xsu} is required as the resistive open increases in order to have a logic error. The obtained values of t^*_{xsu} are of several nanoseconds for moderate resistive opens.

Opens in the output inverter of the master latch

The resistive opens in the output stage of the master latch have been classified in the same way that in the driver stage. They behave similarly. In addition, opens located in the output inverter of the master latch, except multiple open gates, are affected by charge sharing. Champac et al. [83] have also observed charge sharing in the symmetric flip-flop for single floating gate defects. This effect helps for a logic error to appear in the defective flip-flop. Charge sharing effect takes place when the input stage of the slave latch closes (See Figure 3.45).

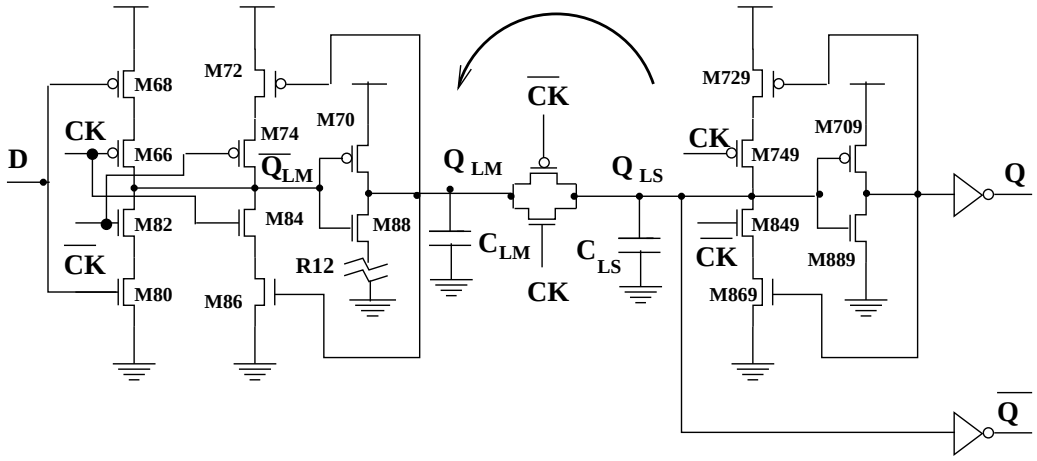


Figure 3.45: Effect of charge sharing.

Let's analyze resistive open R_{12}. A first vector D=1 is initially applied. Then a second vector T2 (D=0) evaluates the open defect. This second vector discharges the output node of the master latch Q_{LM} (See Figure 3.45) through the defective path. Charge sharing effect takes place for the second vector when the master latch changes to the memory phase. In memory phase, the transmission

gate is closed (See Figure 3.42). Then, the stored charge in the capacitance at the output of the master latch C_{LM} and the stored charge in the capacitance at the output of the slave latch C_{LS} is shared between them. The final state of the latch is determined by the voltages at nodes Q_{LM} and $\overline{Q_{LM}}$ after charge sharing and the input/output transfer characteristics of the inverters in the feedback loop [89] [83] [97].

The impact of charge sharing is an increment on the time t^*_{xsu} (See Figure 3.46). Cases for charge sharing (cs) and no charge sharing (no_cs) are shown. Higher $t_{xsu}*$ times for charge sharing cases are obtained than those observed for the non-charge sharing cases. A higher value of t^*_{xsu} makes the open easier to detect.

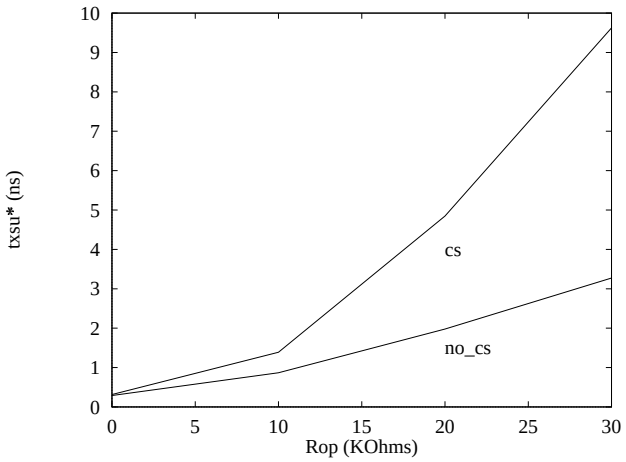


Figure 3.46: t^*_{xsu} for the resistive open R_{12}. Case for charge sharing (cs) and case for no charge sharing (no_cs).

A first order analytical expression considering charge sharing effects has been developed. The analysis is divided in two parts. The first part takes into account the writing time of the second vector (D=0) and the partial discharge of node Q_{LM} through the resistive open. The second part considers the memorizing time of the second vector when the charge sharing between nodes Q_{LM} and Q_{LS} takes place.

In the first part, node Q_{LM} is discharged according with the following equation:

$$V_{Q_{LM}}^{bcs} = V_{DD}e^{-t_w/RC_{LM}} \tag{3.4}$$

where $V_{Q_{LM}}^{bcs}$ is the voltage at node Q_{LM} before charge sharing (See Figure 3.45), V_{DD} is the voltage of the power supply, t_w is the writing time of the slave latch for the second vector, R is the value of the resistive open plus the drain to source resistance of the affected transistor, C_{LM} is the related capacitance to node Q_{LM}.

Neglecting the resistance of the TG and conduction through the defective transistor, the voltage at node Q_{LM} after charge sharing is expressed by the following equation:

$$V_{Q_{LM}}^{acs} = \frac{C_{LM}V_{Q_{LM}}^{bcs}}{C_{LM}+C_{LS}} + \frac{C_{LS}V_{Q_{LS}}}{C_{LM}+C_{LS}} \tag{3.5}$$

where $V_{Q_{LM}}^{acs}$ is the voltage in node Q_{LM} after charge sharing, C_{LS} is the related capacitance to node Q_{LS}, $V_{Q_{LE}}$ is the voltage at node Q_{LS} before charge sharing. This voltage has a value of V_{DD}.
The following equation is obtained when equation 3.4 is substituted into equation 3.5:

$$V_{Q_{LM}}^{acs} = \frac{C_{LS}}{C_{LM}+C_{LS}}V_{DD} + \frac{C_{LM}}{C_{LM}+C_{LS}}V_{DD}e^{-t_w/RC_{LM}} \tag{3.6}$$

The output latch will evolve to 1 or 0 logic depending on the voltage $V_{Q_{LM}}^{acs}$ and the input/output transfer characteristics of the two inverters in the memory circuitry.

The capacitance $C_{Q_{LS}}$ is greater than $C_{Q_{LM}}$ in the analyzed symmetric flip-flop cell (See Figure 3.45). There are four gate capacitances and four diffusion capacitances at node $C_{Q_{LS}}$, and two gate capacitances and four diffusion capacitances at node $C_{Q_{LM}}$. This implies that the final voltage after charge sharing

tends to the value of the higher voltage before charge sharing.

The right term in equation 3.6 represents the discharge of node Q during the writing phase of the second vector. The left term represents the voltage at the capacitance C_{LS} before charge sharing. The capacitances C_{LM} and C_{LS} share they charge according to its capacitance values. This is represented by the term to the left in the previous equation. Equation 3.6 clearly shows that the voltage at node $V_{Q_{LM}}$ after charge sharing is higher than the its value before charge sharing assumming equal values of $C_{Q_{LS}}$ and $C_{Q_{LM}}$, because charge sharing, the voltage at node Q_{LM} is equal or greater than $V_{DD}/2$. As a consequence, charge sharing helps for a logic error to appear in the symmetric flip-flop cell.

3.4.3 Analysis in the slave stage

Resistive opens located in the slave latch manifest as additional delay or logic error at the output of the flip-flop. Taking into account the stages in the slave latch, it can be stated:

- The behavior and test conditions for opens located in the clocked and output stages of the slave latch are similar to those found in the same stages of the symmetric CMOS latch.

- The behavior and test conditions for opens located in the driver stage of the slave latch are similar to those found for the input stage of the TG latch.

3.4.4 Summary of the results

The most significative results for opens in the symmetrical flip-flop are:

- The topology of the master latch is similar to the symmetric CMOS latch. Because this, the opens located in the master latch of the symmetrical flip-flop, except those located in the output inverter, behaves similarly to the symmetric CMOS latch. These opens manifest at the flip-flop output as logic errors.

- The opens located at the output inverter of the master latch are influenced by charge sharing. Charge is redistributed at both ends of the TG when the master latch goes to the memory phase. Because this a logic error is more prone to appear at the flip-flop output. The critical t^*_{xsu} is increased indicating that charge sharing makes easier to test these opens respect to the case without charge sharing.

- Opens located in the slave latch manifest as additional delays or logic error at the flip-flop output.

- Opens located in the TG of the driver stage in the slave latch of the symmetrical flip-flop have a similar behavior to that found in the input stage of the TG CMOS latch.

- Opens located in the clocked and output inverter of the slave latch of the symmetrical flip-flop behaves similarly to that found in the same stages of the symmetric CMOS latch.

A summary of the possible exciting transitions for the resistive opens in the master latch and slave latch of the symmetric CMOS flip-flop is given in Table 3.8. The results are only given for opens in the Nmos networks. Opens located in a complementary position in the Pmos network behaves similarly.

In Table 3.9, the output behavior of resistive opens in the symmetric CMOS flip-flop is summarized. Resistive opens affecting the driver and output stage of the master (slave) latch can be mapped to the output as a logic error (delay or logic error). Very high resistive opens affecting the clocked inverter (closing

	Master Latch			*Slave Latch*		
Stage	*Open*	*Testability*	*Vectors*	*Open*	*Testability*	*Vectors*
DS	R_4	DET	0→1	R_{319}	Hard DET	0→1 1→0
	R_{10}	DET	0→1	R_{269}	Hard DET	0→1 1→0
	R_{17}	DET^{ic}	0→1	R_{149}	Hard DET	0→1 1→0
	R_{22}	DET^{ic}	0→1 1→0	R_{299}	DET^{ic}	0→1 1→0
	R_{13}	DET^{ic}	1→0 1→0	R_{289}	DET^{ic}	0→1 1→0
OS	R_5	Non DET	—	R_{59}	Non DET	—
	R_{11}	Non DET	—	R_{119}	Non DET	—
	R_{18}	Non DET	—	R_{189}	Non DET	—
	R_{21}	DET	0→1	R_{219}	Partial DET	0→1
CIS	R_6	DET^{cs}	1→0	R_{69}	DET	0→1
	R_{12}	DET^{cs}	1→0	R_{129}	DET	0→1
	R_{19}	DET^{cs}	0→1 1→0	R_{199}	DET^{ic}	0→1 1→0
	R_{27}	DET	0→1 1→0	R_{279}	DET^{ic}	0→1 1→0

Table 3.8: Summary of the behavior for resistive opens for the symmetric CMOS flip-flop. *ic*: initial condition dependent. *cs*: charge sharing dependent. DS: Driver Stage. OS: Output Stage. CIS: Clocked Inverter Stage.

memory) stage in the master (slave) latches may produce data retention faults. A logic error may also appear for the feedback path of the clocked inverter stage.

Opens	*Master*	*Slave*
Conducting Paths (DS)	logic error	—
Open Gates (DS)	logic error (ic)	—
Conducting Paths[1] (DS)	—	small delay
Conducting Paths[2] (DS)	—	delay or logic error (ic)
Open Gates (DS)	—	delay
Conducting Paths (OS)	logic error (cs)	delay or logic error
Open Gates (OS)	logic error (cs, ic)	delay, logic error (ic)
Conducting Paths (CIS)	drf	drf
Control Path (CIS)	drf	drf
Feedback Path (CIS)	drf, logic error	drf, logic error

Table 3.9: Summary of the results for the symmetric CMOS flip-flop. DS: Driver stage, OS: Output stage, CIS: Clocked inverter stage. drf: data retention fault, (ic): initial condition dependent, (cs): charge sharing dependent. Conducting path[1]: affected one transistor of TG. Conducting path[2]: affected two transistors of TG.

3.5 Analysis in the transmission gate flip-flop

In this section, the behavior of opens in TG latches is extended to TG flip-flops. The analysis is focused to detect timing violations in the defective latch. Timing violations affecting to the next latch respect to the defective one will be analyzed in section 3.6. The influence of charge sharing in the testability of some opens is analyzed.

3.5.1 General topology

In this subsection, the behavior of resistive opens in a transmission gate flip-flop is analyzed. The master and slave latches of the TG flip-flop are TG latches like that previously analyzed in section 3.3. Each latch is composed by the following

stages: input, inverter and closing memory stages. The flip-flop is activated at the positive clock transition.

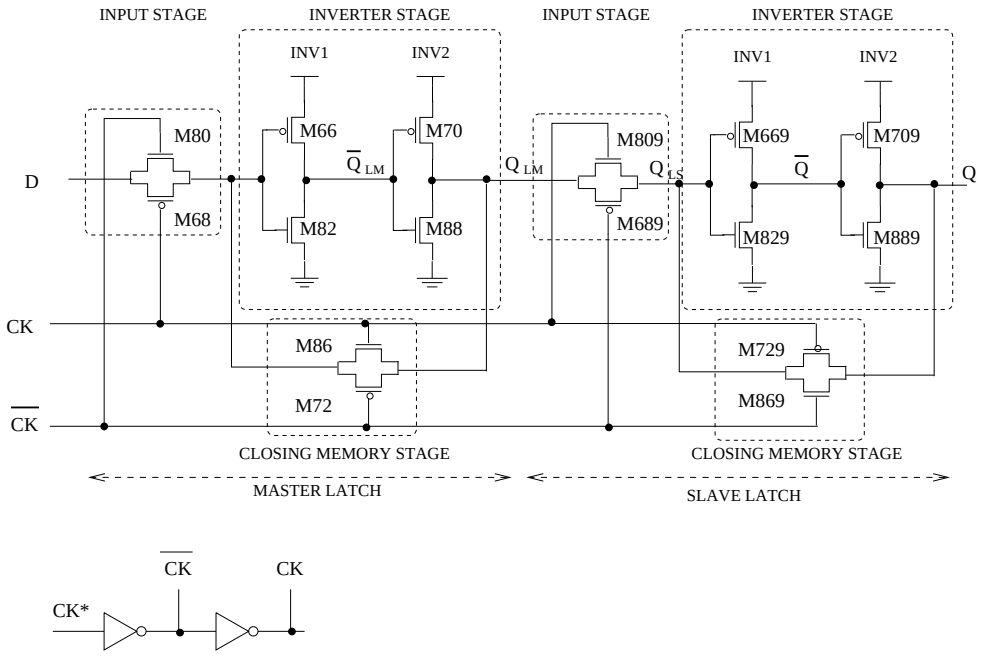


Figure 3.47: Schematic diagram of a transmission gate flip-flop.

The considered open locations are shown in Figure 3.48. The open is modeled as a lumped resistance with a continuous range of values.

The analysis of the TG CMOS flip-flop has been divided in:

a) Analysis in the master latch

b) Analysis in the slave latch

Resistive opens in master latch are analyzed with the parameter t^*_{xsu}. Time t^*_{xsu} is the critical t_{xsu} to observe logic error at the defective latch of the flip-flop. Opens in the slave latch are analyzed with the parameter t^*_{xsu} and by the delay testing conditions.

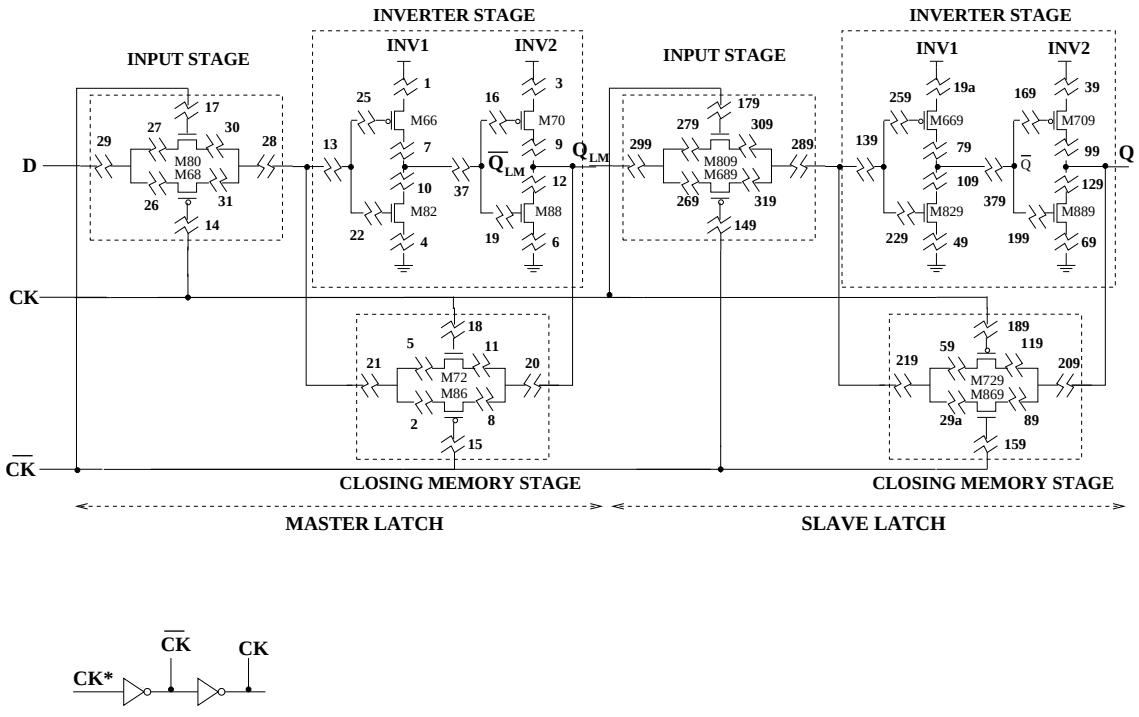


Figure 3.48: Resistive opens in the transmission gate flip-flop.

3.5.2 Analysis in the master latch

Resistive opens in the master latch manifest as logic error at the output of the TG flip-flop when its timing conditions are violated. However, additional delays due to some resistive opens in the master latch could produce timing violations in the next latch. This is analyzed in section 3.6.

Because the structure of the TG flip-flop is the same that of the TG latch, its the behavior is stated as follow:

- Resistive opens at the input stage, closing memory stage and INV1 of the inverter stage (See Figure 3.48) have a similar behavior to that found in the same stages in the TG CMOS latch.

- Resistive opens in INV2 of the inverter stage are influenced by charge sharing.

Resistive opens in the input stage, closing memory stage and INV1 of the inverter stage

Most of the opens in the closing memory stage are not detectable by logic or delay testing. However, some opens in gates could give logic error for high resistive opens and under certain initial conditions. Resistive opens in the input and inverter stages, except those affecting one transistor of the TG, can produce logic error when the critical t^*_{xsu} condition is violated.

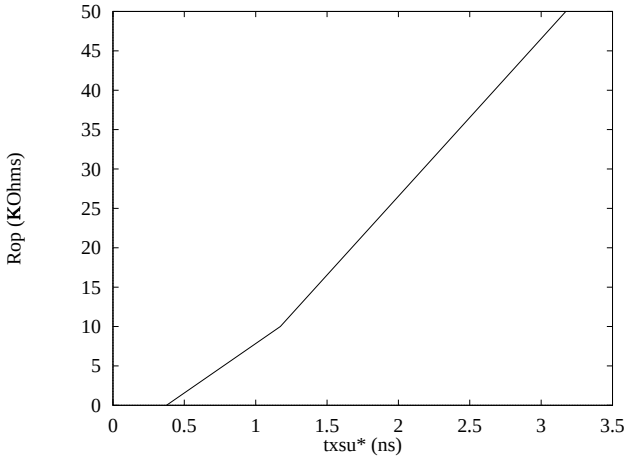


Figure 3.49: t^*_{xsu} for resistive open R_{29}.

Let's analyze resistive open R_{29} located at the input stage of the master latch (See Figure 3.48). This open is excited using a two test vector. A first input data vector D=0 is written and memorized. Then a second input data vector D=1 is applied. Because the open, the current capability through the input transmission gate is decreased. The required t^*_{xsu} for detecting a given resistive open is given in Figure 3.49. Higher resistive opens produce higher critical time t^*_{xsu} (See Figure 3.49). Logic testing can be used to test opens in the conducting path. In addition, high values of resistive opens in R_{29} depend on the initial condition as previously stated.

Resistive opens in the inverter (INV2) stage

Opens in inverter INV2 of the inverter stage, except multiple open gates, are affected by charge sharing (See Figure 3.48). Two effects of charge sharing can be observed for opens in the inverter INV2. The first charge sharing effect is between the output of the master latch Q_{LM} and the voltage at node D' (See Figure 3.50). The second charge sharing effect is between Q_{LM} and Q_{LS}.

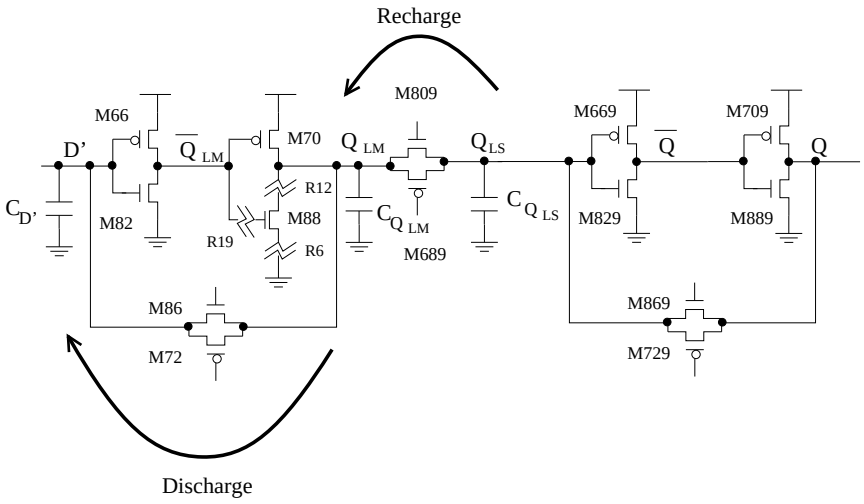


Figure 3.50: Charge sharing effect.

Suppose that a high logic data is written for the first vector. Nodes D', Q_{LM}, Q_{LS} are charged to high logic level. Then, the second vector applies a low logic level D=0 is but node D' follows to input node D during the writing phase of the second vector. Node Q_{LM} tries to follow node D but due to the resistive open node Q_{LM} is not completely discharged. When the master (slave) latch goes to the memory (writing) phase, the two charge sharing occur:

a) Nodes D' and Q_{LM} are connected through the transmission gate. The voltage at both nodes is shared. This means that the voltage at node Q_{LM} is lowered (discharged). This effect tends to mask the resistive open.

b) Nodes Q_{LM} and Q_{LS} are interconnected. Node Q_{LM} is recharged because node Q_{LS} has a high logic level before charge sharing. The final voltage at node Q_{LM} tends to a high logic level. The final state of the latch is determined by the voltages at nodes Q_{LM} and Q_{LM} after charge sharing and the input/output

transfer characteristics of the inverters in the feedback loop [89] [83] [97].

Let's analyze resistive open R_{12} (See Figure 3.48). The resistive open is excited by a two test vector. The first vector D=1 initializes the flip-flop to high logic value. Then the second vector D=0 tries to toggle the state of the flip-flop to low logic value. Node Q_{LM} should be discharged through transistor M88 however the resistive open is opposed to any change in node Q_{LM}. Discharge time of node Q_{LM} is increased because the effect of the resistive open. Charge sharing effect can result as consequence of the resistive open (See Figure 3.51).

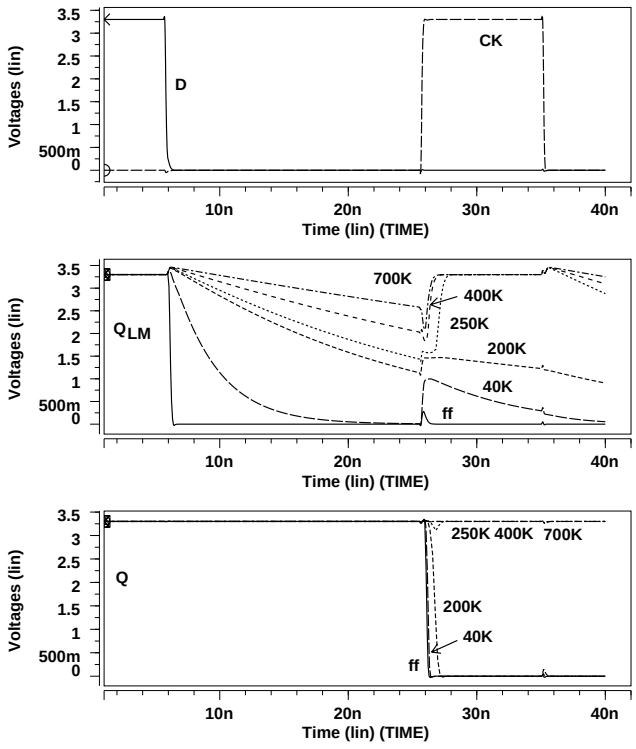


Figure 3.51: Charge sharing effect for resistive open R_{12}. Upper panel.- clock CK and data D signals. Middle panel.- node Q_{LM}. Lower panel.- node Q.

In the upper panel, the signals at nodes D and CK are given. Transition data 1→0 is the condition of two test pattern vector. In the middle panel, the voltage at node Q_{LM} for 250KΩ, 200KΩ, 40KΩ and fault-free cases are shown. At the beginning of memory phase charge sharing takes place. Small resistive opens

evolve slowly to the correct logic level. However for resistive opens of 250KΩ and higher, a logic error is produced. For those cases the timing condition t^*_{xsu} is violated.

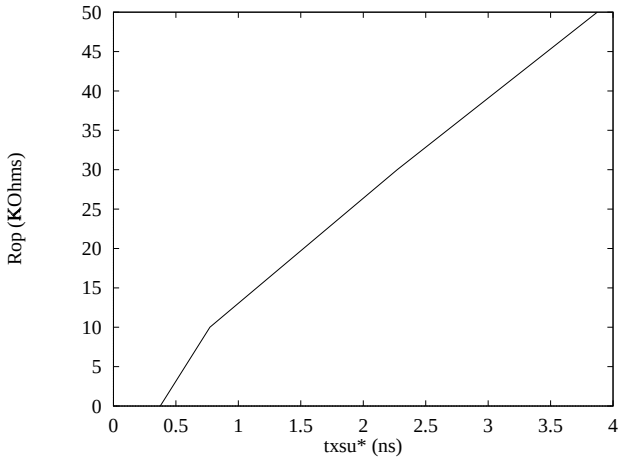


Figure 3.52: t^*_{xsu} for resistive open R_{12}.

The critical time t^*_{xsu} as function of the value of the resistive open is shown in Figure 3.52. Higher resistive opens require higher t^*_{xsu} in order to detect the open.

A first order analytical expression has been developed to estimate the voltage at node Q_{LM} after charge sharing. The discharge part is modeled by the following equation:

$$V^{bcs}_{Q_{LM}} = V_{DD} e^{-t_w / RC_{Q_{LM}}} \tag{3.7}$$

where $V^{bcs}_{Q_{LM}}$ is the voltage at node Q_{LM} before charge sharing, V_{DD} is the voltage at node Q_{LM} due to the applied first vector, t_w is the writting time of the master latch for the second vector, $C_{Q_{LM}}$ is the capacitance of the node Q_{LM}, R is the open resistance plus drain to source resistance of transistor M88 (See Figure 3.50).

Charge sharing takes place when the master (slave) latch goes to the memory (writing) phase. Two charge sharing mechanisms occur (See Figure 3.50): a)

discharge through the transmission gate in the feedback loop of the master latch, and b) recharge through the transmission gate of the input stage of the slave latch. Taking this into account, the voltage at node Q_{LM} after charge sharing, neglecting the transmission gate resistance and the current path through the defective transistor, can be estimated by:

$$V_{Ql}^{acs} = \frac{C_{Ql}V_{Ql}^{bcs} + C_{\overline{Q'}}V_{\overline{Q'}}}{C_{Ql} + C_{D'} + C_{\overline{Q'}}} \tag{3.8}$$

where $V_{Q_{LM}}^{acs}$ is the voltage at node Q_{LM} after charge sharing, $C_{D'}$ is the capacitance of node D', $C_{Q_{LS}}$ is the capacitance of node Q_{LS}, $V_{Q_{LS}}$ is the voltage at node Q_{LS}.

After substituting equation 3.7 into equation 3.8, the following equation results:

$$V_{Q_{LM}}^{acs} = \frac{V_{DD}C_{Q_{LM}}e^{\frac{-t_w}{RC_{Q_{LM}}}} + V_{DD}C_{Q_{LS}}}{C_{D'} + C_{Q_{LM}} + C_{Q_{LS}}} \tag{3.9}$$

It must be noted that a voltage $V_{Q_{LM}}^{acs}$ will produce a corresponding voltage $\overline{V_{Q_{LM}}^{acs}}$ for the other inverter in the memory circuitry (See Figure 3.50). The output latch will evolve to 1 or 0 logic depending on the voltage $V_{Q_{LM}}^{acs}$ and the input/output transfer characteristics of the two inverters in the memory circuitry.

Let's represent the voltage given by equation 3.7 as:

$$V_{DD}e^{-t_w/RC_{Q_{LM}}} = \alpha V_{DD} \tag{3.10}$$

Substituting the previous equation in 3.9 a simplified equation of 3.10 is obtained:

$$V_{Q_{LM}}^{acs} = \frac{\alpha V_{DD}C_{Q_{LM}} + V_{DD}C_{Q_{LS}}}{C_{D'} + C_{Q_{LM}} + C_{Q_{LS}}} \tag{3.11}$$

The capacitances at nodes D', Q_{LM} and Q_{LS} have similar values in the analyzed transmission gate flip-flop. There are two gate and four diffusion capacitances at node D'. For the node, Q_{LM} there are six diffusion capacitances. For the node Q_{LS}, there are two gate and four diffusion capacitances. Assuming equal capacitance values at the nodes D', Q_{LM} and Q_{LS} the following expression is obtained:

$$V_{Q_{LM}}^{acs} = \frac{\alpha + 1}{3} V_{DD} \tag{3.12}$$

From the previous expression, it can be stated that the combined effect of charge sharing depends on the voltage at node Q_{LM} (modeled by α in equation 3.10) before charge sharing:

- For α=0.5, both charge sharing mechanisms cancel each other. This means the voltage after charge sharing is the same than before charge sharing. The voltage after charge sharing is similar to the value before charge sharing for α values close to 0.5.

- For α greater that 0.5, the voltage after charge sharing is lower than the voltage before charge sharing. In this case, charge sharing makes the open more difficult to detect.

- For α lower than 0.5, the voltage after charge sharing is greater than the voltage before charge sharing. In this case, charge sharing makes the open easier to detect.

3.5.3 Analysis in the slave latch

Resistive opens located in the slave stage manifest as additional delays or logic error at the output of the TG flip-flop in a similar way that opens in the simple TG latch.

3.5.4 Summary of the results

Some important items can be derivated from the analysis in TG flip-flop cell, among them we can mention the followings:

- Opens located in the slave latch of the TG flip-flop have a similar behavior to that found in the TG CMOS latch cell. They can be detected by delay or logic testing.
- The topology of the master latch of the TG flip-flop is similar to the TG CMOS latch cell. Because this, the defects located in the master latch of the TG flip-flop, except those located in the inverter INV2 of the inverter stage, behaves similarly to the TG CMOS latch. These defects can be detected by logic testing.
- Defects located at the inverter INV2 of the inverter stage of the TG flip-flop are influenced by charge sharing effects. Charge sharing takes place when the phase memory of the master latch begins. Double charge sharing effects occur: recharge and discharge.
- Charge sharing can make the open easier or more difficult to detect. Among other things, this depends on the voltage conditions before charge sharing to occur.

A summary of the test vector to test resistive opens in the master and slave latches is summarized in Table 3.10. The results are given for opens in the Nmos transistors. Similar behavior can be observed for opens in the Pmos transistors. The cases labeled as DET^{ic} correspond to opens initial conditions dependent. The cases labeled as DET^{cs} are those affected by charge sharing.

Table 3.11 shows the output behavior for resistive opens in the master and slave latches of the TG flip-flop. Most resistive opens affecting the master latch (slave) can be mapped to the output as a logic error (delay or logic error). Opens affecting one transistor of the TG in the closing memory stage of the master and slave latches do not produce either logic or delay error. Very high resistive opens affecting both transistors of the TG in the closing memory stage of the master

	Master Latch			*Slave Latch*		
Stage	*Open*	*Testability*	*Vectors*	*Open*	*Testability*	*Vectors*
IS	R_{29}	DET^{ic}	0→1 & 1→0	R_{299}	DET^{ic}	0→1 & 1→0
	R_{28}	DET^{ic}	0→1 & 1→0	R_{289}	DET^{ic}	0→1 & 1→0
	R_{27}	Hard DET	0→1 & 1→0	R_{279}	Hard DET	0→1 & 1→0
	R_{30}	Hard DET	0→1 & 1→0	R_{309}	Hard DET	0→1 & 1→0
	R_{17}	Hard DET	0→1 & 1→0	R_{179}	Hard DET	0→1 & 1→0
INVS	R_{13}	DET^{ic}	0→1 & 1→0	R_{139}	DET^{ic}	0→1 & 1→0
	R_{37}	DET^{ic}	0→1 & 1→0	R_{379}	DET^{ic}	0→1 & 1→0
	R_{19}	DET^{cs}	0→1 & 1→0	R_{199}	DET^{cs}	0→1 & 1→0
	R_{22}	DET^{ic}	0→1 & 1→0	R_{229}	DET^{ic}	0→1 & 1→0
	R_4	DET	0→1	R_{49}	DET	0→1
	R_{12}	DET^{cs}	1→0	R_{129}	DET^{cs}	1→0
	R_{10}	DET	0→1	R_{109}	DET	0→1
	R_6	DET^{cs}	1→0	R_{69}	DET^{cs}	1→0
CMS	R_{20}	Non DET	—	R_{209}	Non DET	—
	R_{21}	Non DET	—	R_{219}	Non DET	—
	R_2	Non DET	—	R_{29a}	Non DET	—
	R_8	Non DET	—	R_{89}	Non DET	—
	R_{15}	Hard DET	0→1	R_{159}	Hard DET	1→0

Table 3.10: Summary of behavior for resistive opens in the master latch and slave latch. *cs*: charge sharing dependent, *ic*: initial condition dependent. IS: Input Stage. INVS: Inverters Stage. CMS: Closing Memory Stage.

and slaves latches may produce data retention faults.

Opens	*Master*	*Slave*
Conducting Path[1] (IS)	no error	small delay
Conducting Path[2] (IS)	logic error (ic)	delay or logic error (ic)
Open Gates (IS)	logic error (ic)	logic error or delay (ic)
Control Path (CMS)	logic error (ic)	logic error or delay (ic)
Conducting Path[1] (CMS)	no error	no error
Conducting Path[2] (CMS)	data retention fault	data retention fault
Conducting Path (INV1 of INVS)	logic error	delay or logic error
Open Gates (INV1 of INVS)	logic error (ic)	delay or logic error (ic)
Conducting Path (INV2 of INVS)	logic error (cs)	delay or logic error (cs)
Open Gates (INV2 of INVS)	logic error (ic, cs)	delay or logic error (ic, cs)

Table 3.11: Summary of behavior for resistive opens in the master latch and slave latch of the TG flip-flop. IS: Input Stage , INVS: Inverter Stage, CMS: Closing Memory Stage, Conducting Path[1]: affected one transistor of the TG, Conducting Path[2]: affected both transistor of the TG. (cs): charge sharing dependent, (ic): initial condition dependent.

3.6 Analysis in a scan path chain

In this section, testability and timing test conditions for resistive opens in a scan path chain are analyzed. It is analyzed a scan path chain composed by three flip-flop (See Figure 3.53). The multiplexer stage at the input of the scan cells has not been considered to make simple the analysis. Each flip-flop is composed by two CMOS latches. They can be symmetrical CMOS D latches as those in Figure 3.3 or TG CMOS latches as those in Figure 3.21. The flip-flops are sensitive to rise transitions.

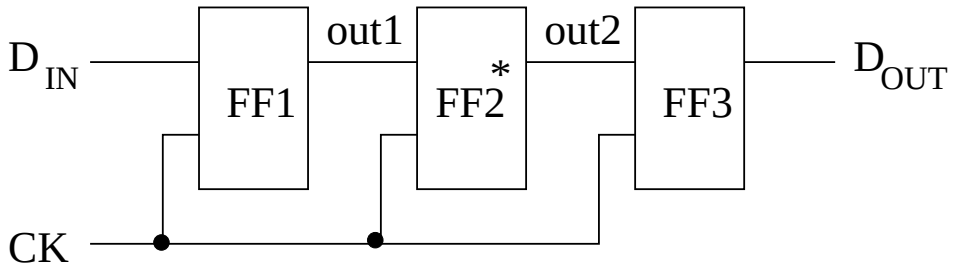


Figure 3.53: Scan path circuit.

Resistive opens in the scan path chain can be located in the master latch or slave latch of each flip-flop. Opens in a scan path chain, except those located in the slave latch of the last flip-flop in the chain, manifest as logic errors at the scan output. The slave latch of the last flip-flop of the scan path chain is the only one manifesting as error logic or delay at the scan output.
Open defects located in the second flip-flop (FF2*) of the scan path chain (See Figure 3.53) are analyzed. The analyzed cases of resistive opens are shown in Figures 3.54 and 3.55 for the cases of symmetric flip-flop and TG flip-flop respectively.

An open located in a latch in the scan chain can produce a logic error at:

- The same defective latch of the flip-flop
- In the next latch connected to the defective one

Conditions for opens producing a logic error in the same defective latch have

been analyzed in the previous subsections. Additionally, some opens in the slave latch of the defective flip-flop can not produce a logic error at the output of the slave latch but they can violate the timing conditions of the fault-free latch of the next flip-flop. A similar behavior can also occur when the open is located in the master latch and the timing conditions of the slave latch of the same flip-flop are violated.

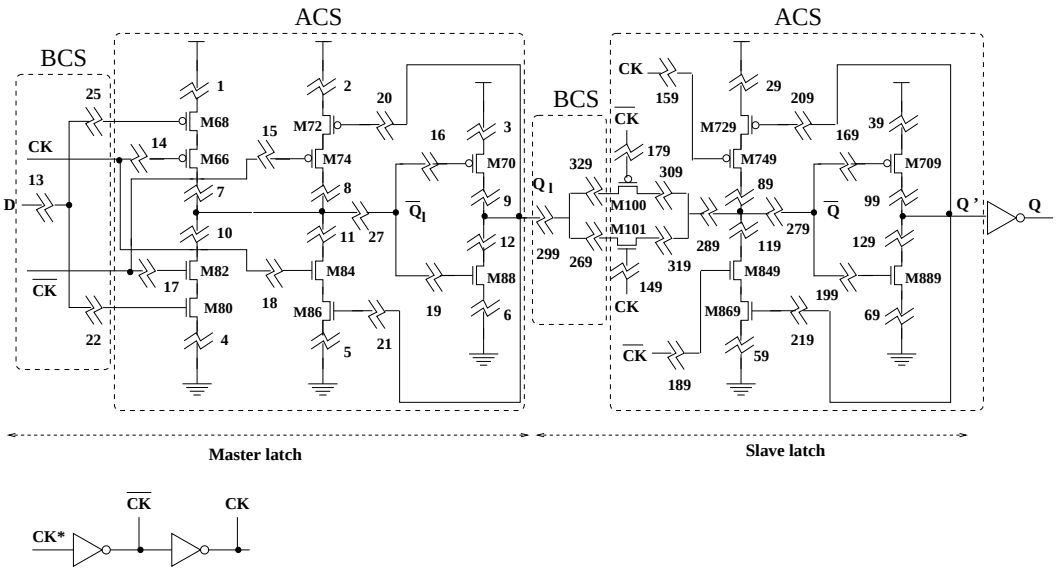


Figure 3.54: Opens in a symmetric CMOS flip-flop.

Resistive opens affecting the second flip-flop (FF2) of the scan path chain (See Figure 3.53) are considered. These opens are excited through the flip-flop FF1. Then the output of FF2 is propagated to the scan output. The analysis for opens affecting a flip-flop in a scan path chain has been carried-out as follows:

- Resistive opens after the clocking signal of the input stage (ACS)
- Resistive opens before the clocking signal of the input stage (BCS)
- Resistive opens producing logic error in the next latch

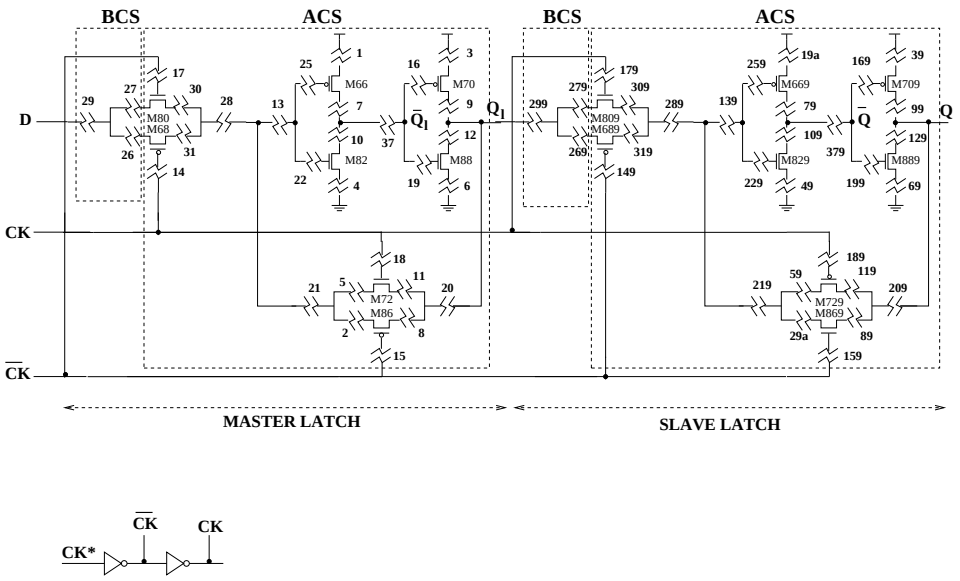


Figure 3.55: Opens in a TG CMOS flip-flop.

Resistive opens after the clocking signal of the input stage (ACS)

These opens are located after the transistors driven by the clock signals in each stage of the flip-flop (See Figure 3.54 and 3.55). Opens affecting the transistor driven by the clock signals are also considered in this group. Because the opens are located after those transistors driven by clock signals only half clock cycle is available to detect these opens (See Figure 3.56). The input data begins to propagate through the resistive open only when the affected latch is in the writing phase (See Figure 3.56). For opens in the master latch (slave latch), time t_{xsu} is defined by CK=low (CK=high). If CK=low (CK=high) is smaller than t^*_{xsu} then a logic error occurs. Equations 3.13 and 3.14 give the conditions for a logic error to occur:

$$t^{low}_{CK} < t^*_{xsu} \qquad Master \;\; latch \tag{3.13}$$

$$t^{high}_{CK} < t^*_{xsu} \qquad Slave \;\; latch \tag{3.14}$$

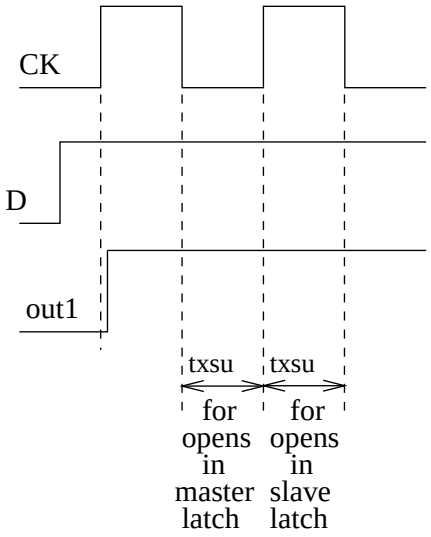


Figure 3.56: Timing diagram for resistive opens located after the clocking signal of the flip-flops.

Resistive opens before the clocking signal of the input stage (BCS)

These opens are located before those transistor driven by the clock signals in the input stage of each latch of the flip-flop (See Figures 3.54 and 3.55). Two cases can be observed for opens before the clock signals: a) opens in the input stage of the master latch (See Figure 3.57 incise a), and b) opens in the input stage of the slave latch (See Figure 3.57 incise b). For both cases, the input data D is available to propagate through the resistive open during the memory phase of the affected latch.

Let's see first the case of opens in the master latch of FF2 (See Figure 3.53). The input voltage of flip-flop FF2 (V_{out1}) begins to propagate through the open in the rising edge of the clock signal (See Figure 3.57). It is propagated through the open when the defective latch is in the memory phase. Then, the data continue its propagation during the writing phase. The timing condition for a logic error to appear due to opens BCS in the master latch is given by:

$$t_{CK}^{low} + t_{CK}^{high} - t_p < t_{xsu}^{*} \tag{3.15}$$

where t_{CK}^{low} (t_{CK}^{high}) is the time that CK remains low (high), t_p is the propagation

delay of the slave latch of the previous fault-free flip-flop of the scan path chain. Equation 3.15 is a first order expression. This equation clearly shows the dependence of the behavior of the defective structure with opens BCS on the full clock cycle. A more accurate expression should take into account the fact that the TG is opened during charging of the right end of the resistance.

In a similar way the timing condition for a logic error to appear due to opens BCS in the slave latch is given by:

$$t_{CK}^{low} + t_{CK}^{high} - t_p < t_{xsu}^{*}$$

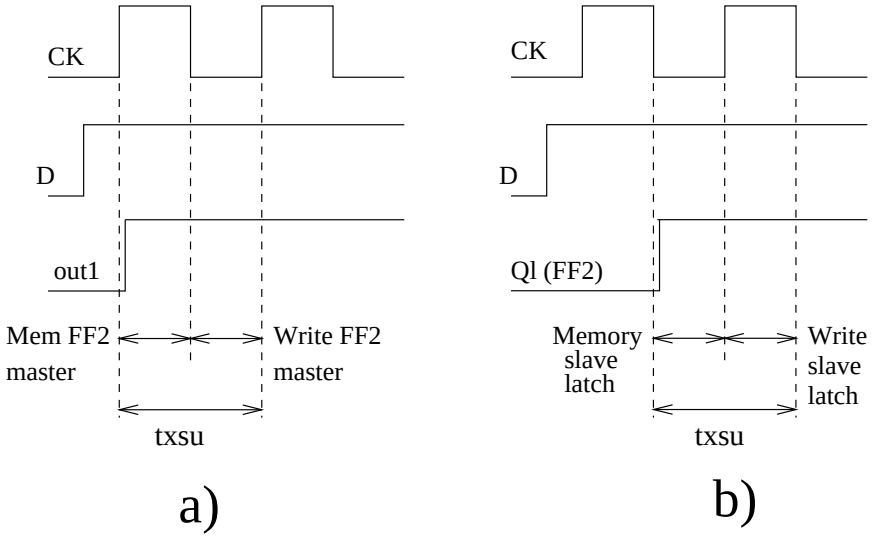


Figure 3.57: Timing diagram for resistive opens located before the clocking signal of the flip-flops. a) opens in the master latch, b) opens in the slave latch.

Resistive opens producing logic error in the next stage

In the previous subsections, it was found that a resistive open in the master (slave) latch can produce an additional delay at the output node of the affected latch without giving a logic error at the defective stage. For a fault-free scan path chain (See Figure 3.53), the output of FF2 changes its state by the positive clock transition after the proper delay propagation of the latch of the previous flip-flop in the chain. For a defective flip-flop, a delay increment is expected.

If the observed delay at the output of FF2 is large enough then it is possible that the timing condition for flip-flop FF3 could be violated and a logic error to appear (See Figure 3.58). It should be noted that the master latch of FF3 is in memory phase after the rising transition of the clock (for CK=0). If the delay at the output of the flip-flop FF2 is smaller than the time CK is low then no logic error appear for FF3. The timing condition for an open in the slave of FF2 to produce a logic error in the next stage is given by:

$$t_d^f > t_{cycle} - t_{su} \tag{3.16}$$

where t_{su} is the set-up time of the next fault-free flip-flop, t_d^f is the delay of the defective slave latch, t_{cycle} is the clock cycle $(t_{CK}^{low} + t_{CK}^{high})$.

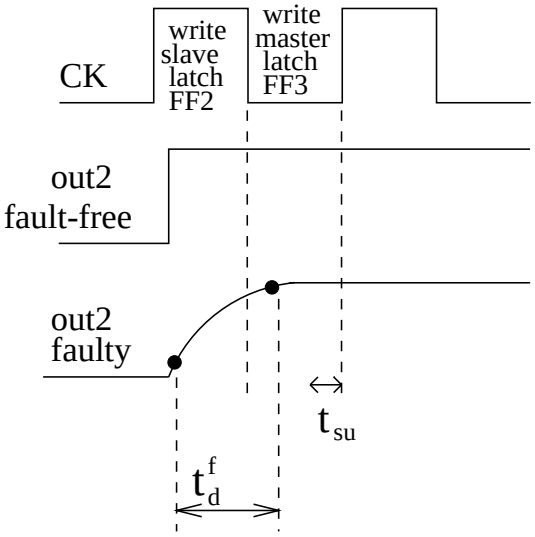


Figure 3.58: Timing diagram for resistive opens producing logic error in the next stage.

3.6.1 Results for the symmetric flip-flop

In this subsection, simulation results to illustrate the behavior and timing conditions for opens in a symmetric flip-flop of a scan path chain are presented. Additionally, the detectability of some opens as function of the clock frequency is also illustrated.

Resistive opens after the clocking signal of the input stage (ACS)

For this case, resistive open R_{12} is analyzed. Resistive open R_{12} is located at the output inverter of the master latch (See Figure 3.54). The timing conditions for this open are defined by equation 3.13. The simulation results are shown in Figure 3.59. In the first panel, the data signal D and clock CK are shown. A first vector D=1 initialize the output node of the master latch (node Q_l in Figure 3.54) of flip-flop FF2* (See Figure 3.53) to a high logic level (See Figure 3.59). Then, a second vector D=0 is applied. In the second panel, the output signal V_{out1} of flip-flop FF1 is shown. V_{out1} changes to 0 logic for the first positive clock transition. Due to the second applied vector, node Q_l is discharged slowly through the resistive open R_{12}. In the third panel, the output of the master latch (V_{Ql}) of defective flip-flop FF2 is shown. V_{Ql} is given for resistive opens of 50KΩ, 24KΩ and fault-free cases. Resistive opens of 24KΩ or larger produce logic error. The time that the clock CK is at low level allows correct behavior for resistive opens lower than 24 KΩ. The output of FF2 is shown in the bottom panel.

The detectability of resistive open R_{12} as function of the frequency of the clock signal (See Figure 3.60) has been obtained. A symmetric clock is used (0.5 of duty cycle). Higher (lower) clock frequencies are needed for smaller (larger) values of resistive opens. For resistive opens higher than a certain value (about 30 Kohms in Figure 3.60), the required frequency to detect the opens decreases significantly. This is because the charge sharing effect dominates the behavior of the defective latch. This effect helps for a logic error to appear in the master latch of flip-flop FF2. In other words, charge sharing makes easier to detect these opens.

Resistive opens before the clocking signal of the input stage (BCS)

Resistive open R_{13} is the case considered to observe the timing condition given by equation 3.15. Resistive open R_{13} is located at the input of the flip-flop (See Figure 3.54). Its timing condition for a logic error is given by $t_{CK}^{low}+t_{CK}^{high}-t_p < t_{xsu}^*$. Simulation results are given in Figure 3.61. In the first panel, clock CK and data D signals are shown. Output of flip-flop FF1 (V_{out1}) is shown in the second panel. In the third panel, the voltage at the node affected by the resistive open (right

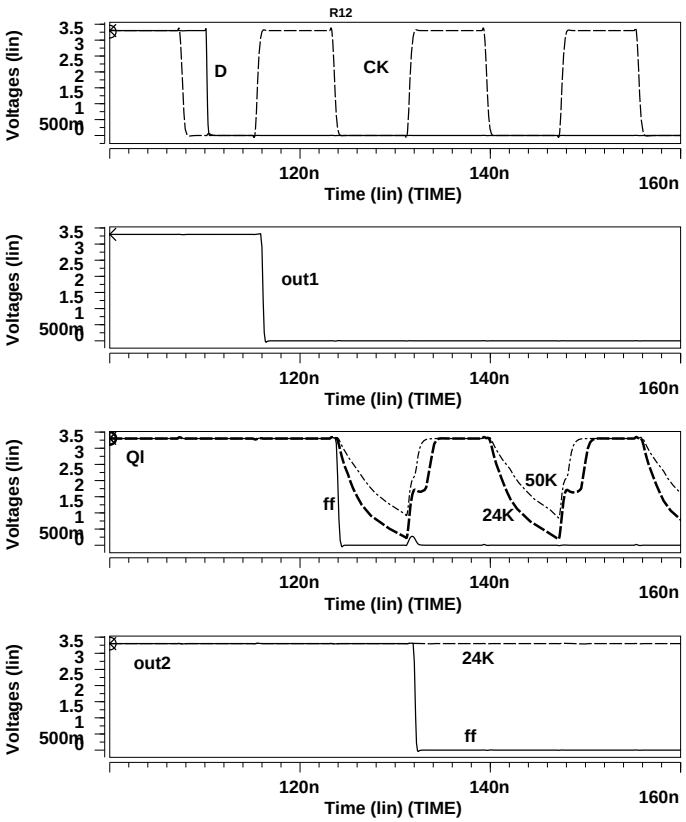


Figure 3.59: Resistive open R_{12}. First panel.- Nodes CK and D. Second panel.- output of flip-flop FF1. Third panel.- master latch output of flip-flop FF2. Fourth panel .- output of flip-flop FF2.

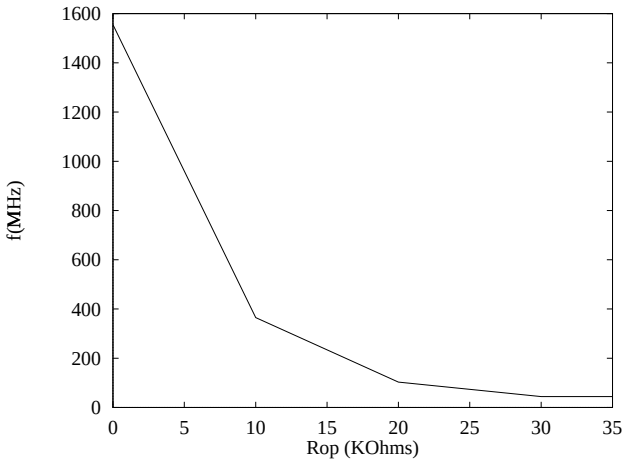


Figure 3.60: Resistive open R_{12} as function of the frequency.

end of the resistance) is shown. This is the actual input to flip-flop FF2. This voltage begins to charge when the master latch of FF2 is in the memory phase (t_{CK}^{high}). Once in the writing phase of the master latch (t_{CK}^{low}), the defective node continues charging. In the fourth panel, the output voltage of flip-flop FF2 is shown. Resistive opens of 500KΩ or higher produce logic error. Resistive opens lower than 500KΩ do not produce logic error.

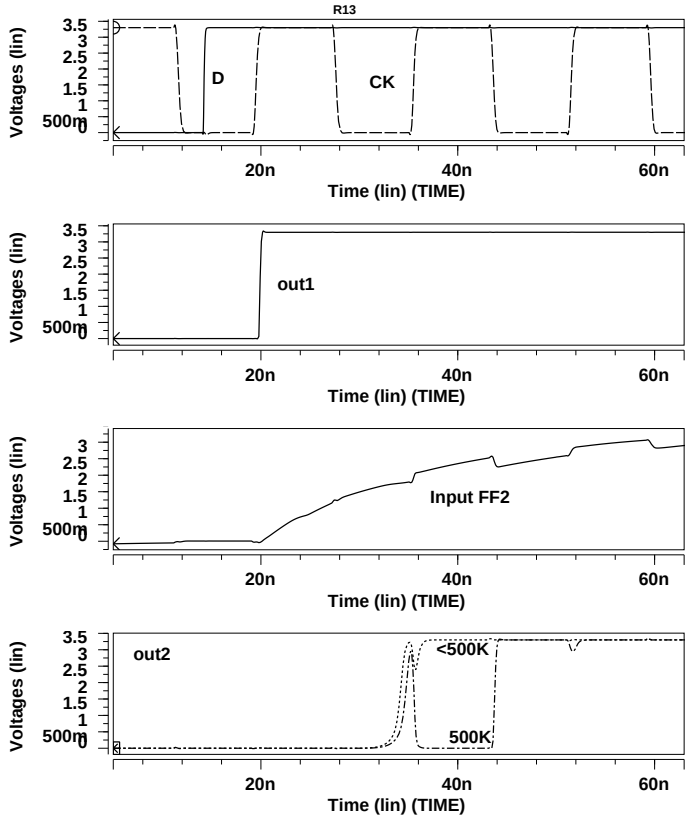


Figure 3.61: Resistive open R_{13}. First panel.- data D and clock CK. Second panel.- flip-flop FF1 output. Third panel.- faulty node voltage. Fourth panel.- flip-flop FF2 output.

Resistive opens producing a logic error in the next flip-flop

Fault R_{129} is the analyzed case for illustrating a logic error in the next fault-free flip-flop. Resistive open R_{129} is located at the output stage of the slave latch (See Figure 3.54). It is analyzed the case when this open does not produce logic error in the defective flip-flop but the timing conditions of the next fault-free flip-flop are violated. As a consequence, a logic error is produced. The timing

condition for a logic error to appear in the next flip-flop for this open is given by equation 3.16. Simulation results are shown in Figure 3.62.

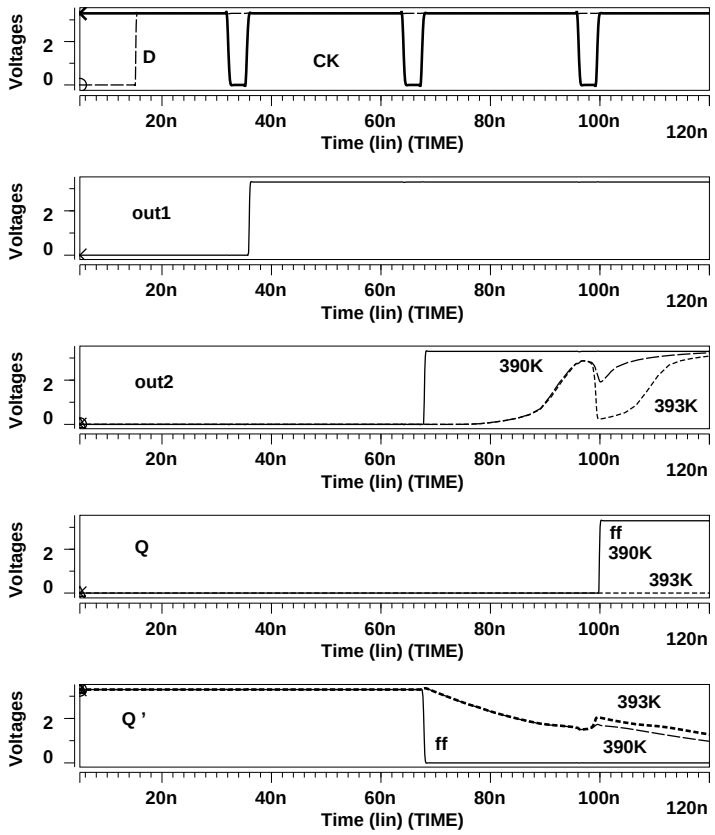


Figure 3.62: Resistive open R_{129} in the symmetric flip-flop. First panel.- data D and clock CK. Second panel.- flip-flop FF1 output. Third panel.- flip-flop FF2 output. Fourth panel.- flip-flop FF3 output. Fifth panel.- node Q'.

In the first panel, data D and clock CK signal are presented. The output voltage of the first flip-flop FF1 is shown in the second panel. In the third panel, the output voltage node V_{out2} of flip-flop FF2 is shown. Defective cases produce large delays at the output of flip-flop FF2. For resistive opens of 390KΩ and lower (higher) data is correctly (not correctly) written and memorized by flip-flop FF3 (See fourth panel). Resistive opens higher than 393KΩ produce logic error. In the fifth panel, the voltage at the output node (Q') of the output stage of the flip-flip FF2 (slave latch) is presented. Fault-free cases change at the second positive clock transition. Faulty cases slowly evolves to low logic level. The cases

are for resistive open of 390KΩ and 393KΩ. Both cases do not present logic error in the defective flip-flop FF2*. However the next flip-flop FF3 fails to write and memorize the data.

Now, it is analyzed the duty cycle requirements for opens producing a logic error in the next stage and with non-logic error in the actual defective stage. It has been found that the opens likely to produce this behavior are those located at the output inverter of the slave latch of the symmetrical flip-flop (See Figure 3.54). The conditions for this behavior to occur are given in Figure 3.63. For many opens an asymmetrical clock duty cycle is required. However, this behavior can also occur for a clock duty cycle close to 0.5 for other opens.

Opens in the input stage or clocked stage of the slave latch are unlikely to present the previous behavior. This is because at the same time that large delays are present at the output the voltages at nodes $\overline{Q}$ and Q' have such values that the latch evolves to the wrong state when memorizing phase of the defective latch starts. Opens in the output stage of the master latch are less likely to present this behavior. This is because charge sharing affecting this stage favors a logic error in the master latch. The behavior of the other opens can be explained in a similar way.

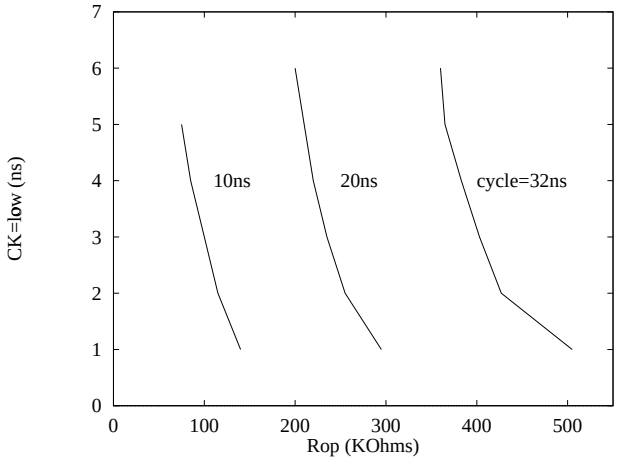


Figure 3.63: Resistive open R_{129} as function of the frequency for the symmetric flip-flop.

3.6.2 Results for TG flip-flop

The three cases shown in the symmetric flip-flop are also illustrated for the TG flip-flop. These cases are:

* Resistive opens ACS.
* Resistive opens BCS.
* Resistive opens producing logic error in the next latch.

A resistive open at the inverter INV2 (R12) of the master latch (See Figure 3.55) is considered for the case of resistive open ACS. This open is considered to compare its detectability with a similar open located in the symmetrical flip-flop. A resistive open affecting one transistor of the TG in the input stage is considered for the case of resistive open BCS. This allows to illustrate the difficulty to detect of this open. This open is also present in the slave latch of the symmetric flip-flop. Finally, the case of a resistive open producing a logic error in the next latch and with non-logic error in the defective flip-flop is presented. The influence of the clock duty cycle is analyzed.

Resistive opens ACS

This open is shown to compare its detectability with resistive open R12 located in the symmetric flip-flop. Resistive open R12 located in the symmetrical flip-flop is affected by charge sharing. For this case charge sharing makes the open easier to detect. Resistive open R12 located in the TG flip-flop is affected by double charge sharing. The resulting effect of the combined charge sharing depends on the voltage before charge sharing as previously stated. The required frequency to detect the open as function of the frequency is shown in Figure 3.64. The required frequency to detect the open increases for lower values of the resistive open. The results for open R12 in the symmetric flip-flop of the scan path chain were shown in Figure 3.60. Comparing Figures 3.60 and 3.64, it can be clearly observed that resistive opens affected by the double charge sharing effect are more difficult to detect that resistive open affected by one charge sharing in the symmetrical flip-flop. This open rules by equation 3.13.

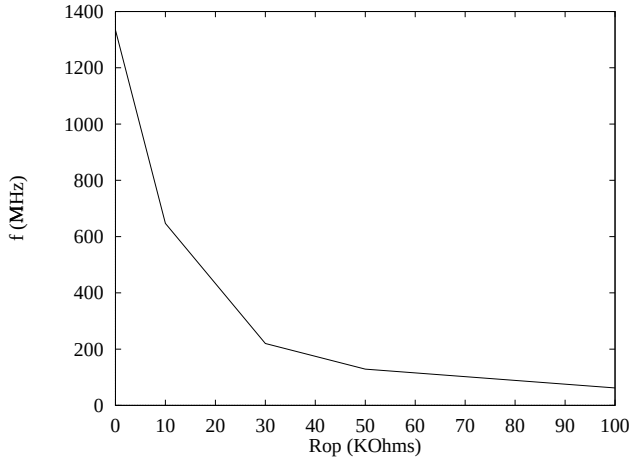


Figure 3.64: Resistive open R_{12} as function of the frequency.

Resistive opens BCS

In the previous sections, it has been stated that these opens are difficult to detect. This open rules by equation 3.15. In Figure 3.65, it is shown the required frequency for detecting open R_{269} (See Figure 3.55) for the scan path chain. Open R_{269} is located at the input stage of the slave latch. For comparison purposes, it is also shown in the same Figure the case for an open in a conducting path of the inverter stage of the master latch (See Figure 3.55). For very high resistive opens are required frequencies above 800 MHz to detect open R_{269} (See Figure 3.65). Frequencies higher than 1 GHz are required for lower values of resistive opens. Hence, it can be stated that this open is difficult to detect. Xu et al. [88] have also found difficult to detect the opens affecting one transistor of the TG. They have proposed to remove the Pmos transistor of the TG.

It should be noted that this type of open is also in the slave stage of the symmetric flip-flop (See Figure 3.54).

Resistive opens producing logic error in the next latch

The analyzed case for the TG flip-flop is R_{129}. Resistive open R_{129} is affecting inverter INV2 of the slave latch (See Figure 3.55). In previous subsections, it has been shown that R_{129} produces large delays. Simulation results are observed in

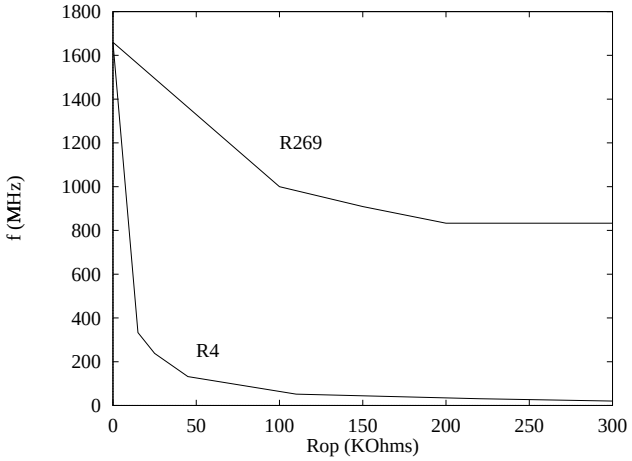


Figure 3.65: Comparison of detectability of R_{269} and R_4.

Figure 3.66.

In the first panel data D and clock CK signals are shown. In the second panel, the output node out1 of flip-flop FF1 is presented. In the third panel, the output node out2 for different resistive opens is shown. From the subsection of TG flip-flops, resistive open R_{129} can produce charge redistribution. The output OUT2 takes longer time to reach well defined logic levels and the delay increases. As a consequence the t_{su} of the next flip-flop can be violated. For this case, resistive open of 60KΩ or higher produce logic error (See fourth panel in Figure 3.66).
It can be seen that opens R_{129} for transmission gate latch based flip-flop requires lower resistive opens to violate the timing condition of the next stage that those observed for symmetric latch based flip-flop. This is because R_{129} produces larger delays in transmission gate latch based flip-flops.

In the transmission gate flip-flop, it has been found that an asymmetrical clock duty cycle is required for opens producing a logic error in the next stage and with non-logic error in the actual defective stage. This is shown in Figure 3.67 for an open in the inverter INV2 of the slave latch (See Figure 3.55). This behavior is less likely to occur for other opens in the transmission gate flip-flop.

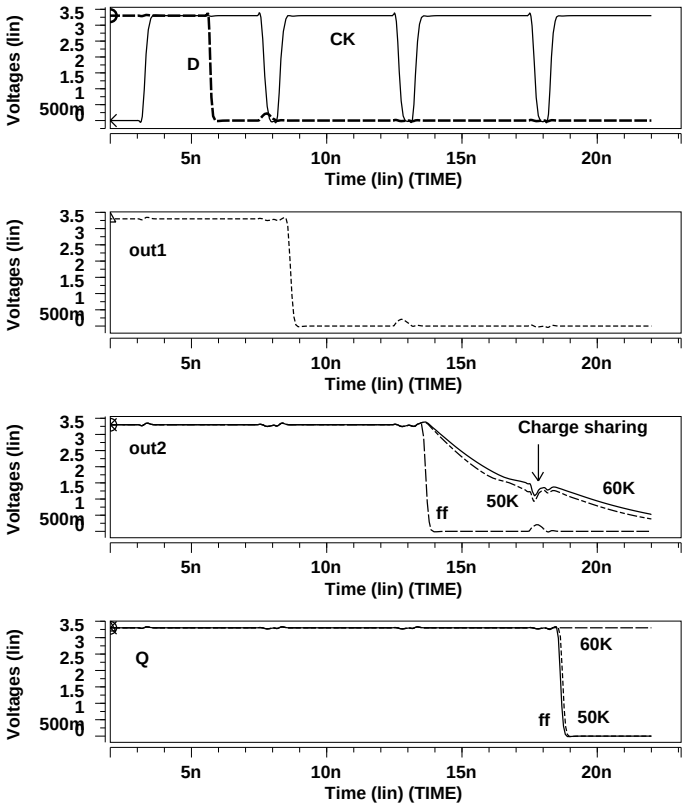


Figure 3.66: Resistive open R_{129} in the TG flip-flop. First panel.- data D and clock CK. Second panel.- flip-flop FF1 output. Third panel.- flip-flop FF2 output. Fourth panel.- flip-flop FF3 output.

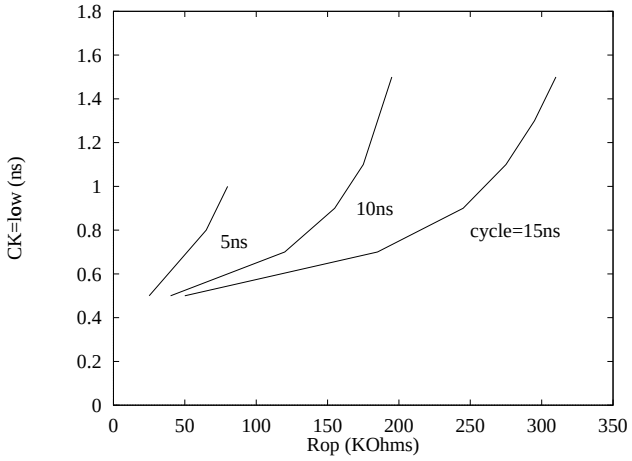


Figure 3.67: Resistive open R_{129} as function of the frequency for the TG latch.

3.6.3 Summary of results

The most significative results for resistive opens in a scan path chain are:

- The behavior of a defective flip-flop as part of a scan path chain has been analyzed. The observed behavior depends on the place that resistive open takes place. Resistive opens that are not located in the last latch of the scan path chain manifest as logic error at the scan output. The last latch of the scan path chain also manifest as an increment of the delay.

- Timing conditions for a logic error to appear have been determined for opens in a scan path chain.

- A logic error can appear in the flip-flop under test as a consequence of violations of the critical t^*_{xsu} in the same flip-flop or violation of the timing conditions of the next fault-free flip-flop in the scan chain.

- For opens located before those transistors driven by the clock signals, a full clock cycle is allowed for writing the input data. Because this, the range of these resistive opens hard to detect is wider in the scan path chain respect to the case of a latch alone. Furthermore, those opens in the conducting path affecting one transistor of the TG of any type of flip-flop are quite hard to detect in the scan path chain.

- For opens located after the transistors driven by the clock signals half clock cycle is allowed for writing the input data. These resistive opens are more likely to be detected respect to the previous case, because only the writing time of the open is considered.

- In a scan chain, violation of the timing conditions of the next fault-free stage without a logic error in the defective latch are mostly met when the duty cycle of the clock is not symmetrical.

- It has been shown that opens affected by double charge sharing effects in the scan path chain are more difficult to detect than opens with only one charge sharing. Double charge sharing affects to the TG flip-flop and one charge sharing affect to the symmetrical flip-flop.

3.7 Experimental Results

In this section, the experimental results for designed and fabricated circuits are presented. Two latches with the proposed DFT circuitries and an scan path chain have been designed and fabricated. DFT circuitries with one control signal and two control signals have been considered. AMS 0.35μm CMOS technology is used. A photograph of the entire integrated circuit has been taken with an electronic microscope (See Figure 3.68).

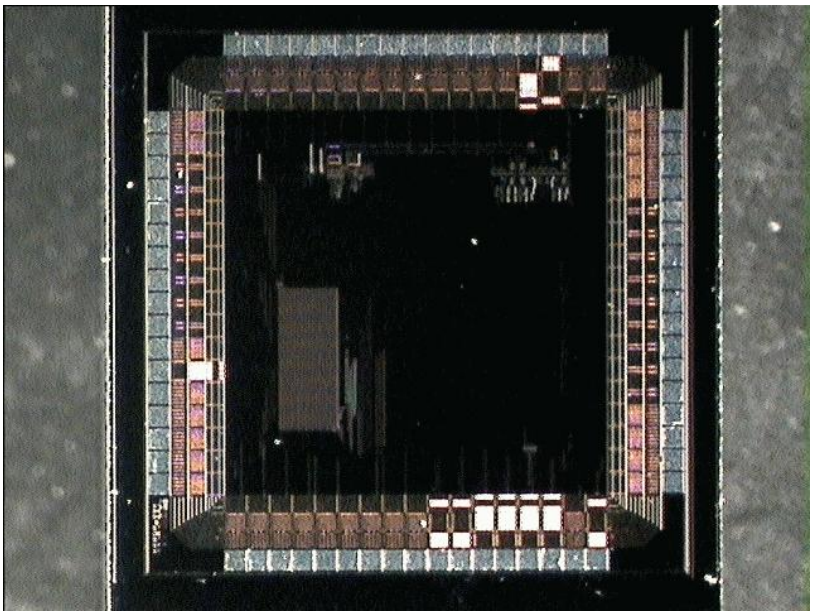


Figure 3.68: Photograph of the entire IC design.

The circuits useful for this thesis are located in the top of the picture. A Tektronix data pattern generator DG2020A has been used to apply the input stimulus to the CUT in the experimental measurements.

3.7.1 DFT proposal: two control signals

The schematic of the symmetric CMOS latch with the DFT two control signals circuitry is shown in Figure 3.69. For memory phase, the DFT circuitry is activated in order to detect opens in the clocked inverter stage. Only opens in the

Nmos network are taken into account. For opens in the Nmos network only the Pmos DFT transistor is activated. Opens have been modeled by transmission gates. The resistance of the opens is modified by controlling the voltages at the gates of each transistor of the transmission gate. The specific values of resistance of the opens in the experimental results have been estimated by simulation. In the simulations were used the voltages applied to the gates of the TG of the CUT. Measuring the voltages at the ends of the transmission gate and the current through it allows to estimate the resistance used during the experimental measurements.

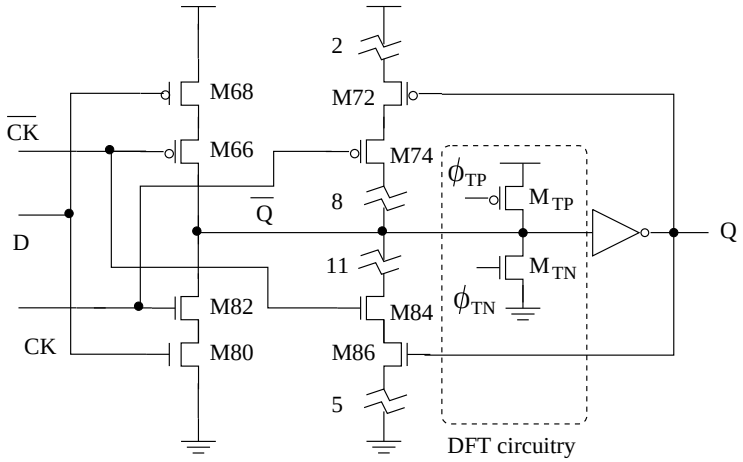


Figure 3.69: Schematic for the testable latch with two control signals.

The DFT circuitry is formed by a Pmos transistor M_{TP} and a Nmos transistor M_{TN} which are driven by control signals ϕ_{TP} and ϕ_{TN}, respectively. These signals are provided from outside of the circuit. The sizes of the DFT transistors are W_P=W_N=1.2μm. A photograph taken with an electronic microscope of the DFT testable latch with two control signals is shown in Figure 3.70. In this photograph is also included the DFT testable latch with one control signal.

The fault-free behavior of the latch is shown in Figure 3.71. Resistive open R_5 has been considered (See Figure 3.69). The input data D of the latch is kept to high logic level (not shown in Figure 3.71). For the memory phase CK=low (See upper curve of Figure 3.71), transistors M84 and M86 are activated and node $\overline{Q}$ is kept low. In memory phase, the Pmos DFT transistor M_{TP} is activated

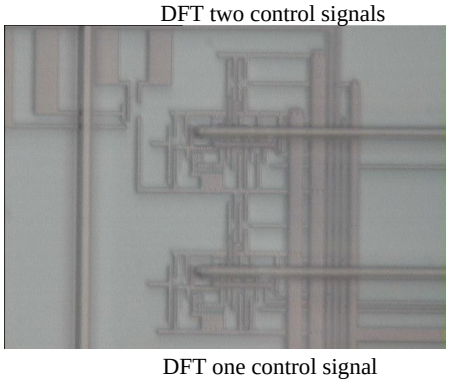


Figure 3.70: Photograph of the fabricated DFT circuitries: two control signal and one control signal.

when ϕ_{TP}=0 (See middle curve of Figure 3.71). A competence between the Pmos DFT transistor and the Nmos network of the clocked inverter takes place. For the fault-free circuit, the logic level of the latch output node Q remains without changes (See lower curve of Figure 3.71).

Figure 3.71: Output of the DFT circuitry for the case of fault-free circuit, T_{wt}=40ns. Upper curve: clock signal CK. Middle curve: activation signal ϕ. Lower curve: output signal Q.

For a defective circuit with R_{open}=∞ the behavior of the DFT circuitry is shown in Figure 3.72. The output of the latch changes to low logic value (lower curve) when the DFT circuitry is activated (middle curve). Hence, the open is detected.

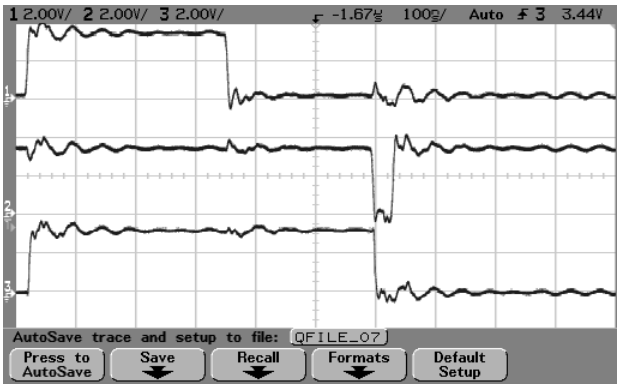


Figure 3.72: Output of the DFT circuitry for the case of R_{open}=∞, T_{wt}=40ns. Upper curve: clock signal CK. Middle curve: activation signal ϕ. Lower curve: output signal Q.

Now, the resistance of open R_5 is varied controlling the voltage at the gates of the transistor of the TG gate. The voltages at the gates of the Pmos (V_P=1.05V) and Nmos (V_N=2.26V) transistors of the TG defines the value of the open. The equivalent resistance is obtained by simulations in HSPICE (R_5=3.0KΩ). A minimum width of the activation signal of 80ns (See middle curve of Figure 3.73) is required to detect the open. Output node changes to low (See Figure 3.73) when the signal ϕ_{TP} is activated and remains low for the rest of the memory phase.

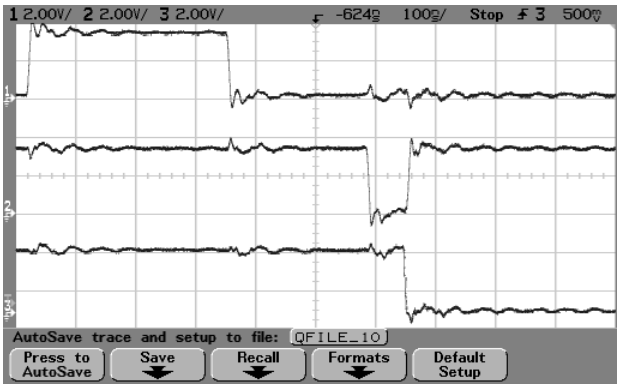


Figure 3.73: Output of the DFT circuitry for the case of R_{open}=3.0KΩ, T_{wt}=80ns. Upper curve: clock signal CK. Middle curve: activation signal ϕ. Lower curve: output signal Q.

For the case of Figure 3.73, signal activation of T_{wt}=80ns is the minimum required width of the activation signal to detect the resistive open. Higher T_{wt}

can detect the same value of resistance. Other values of resistive opens can be detected varying the width of T_{wt}. Some of these measured values are summarized in Table 3.12.

t_{wt} (ns)	R_{op} (KΩ)
10	4.6
40	3.0
80	2.8

Table 3.12: Minimum width of the activation signal t_{wt} used to detect a given resistive open in the clocked inverter stage for the two control signal DFT proposal

It can be observed that a wider T_{wt} is necessary when the resistive open decreases.

3.7.2 DFT proposal: one control signal

The schematic of the latch with the proposed one control signal DFT circuitry is shown in Figure 3.74. The DFT circuitry is used to detect opens in the clocked inverter stage. The Nmos (M_{TN}) and the Pmos (M_{TP}) transistors are symmetrically sized. The designed sizes are W_P=2.7μm and W_N=1.0μm.

The behavior of the latch with the one control signal DFT proposal is shown in Figures 3.75 and 3.76 for fault-free and infinite resistive open, respectively. Input data D is fixed to 1 logic (not shown in Figures 3.75 and 3.76). For the fault-free case input data D=1 is written and memoryzed. In memory phase (CK=low), the DFT circuitry is activated (See middle panel of Figure 3.75) and the output Q remains to a high logic level (See lower panel of Figure 3.75).

For the infinite resistive open case the latch output Q changes to a low logic level (See lower panel of Figure 3.76) when the DFT circuitry is activated. Hence, the open is detected.

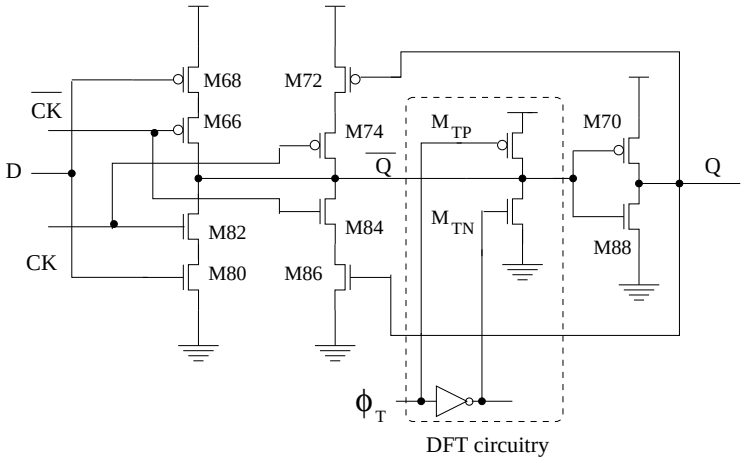


Figure 3.74: Schematic of the testable latch one control signal.

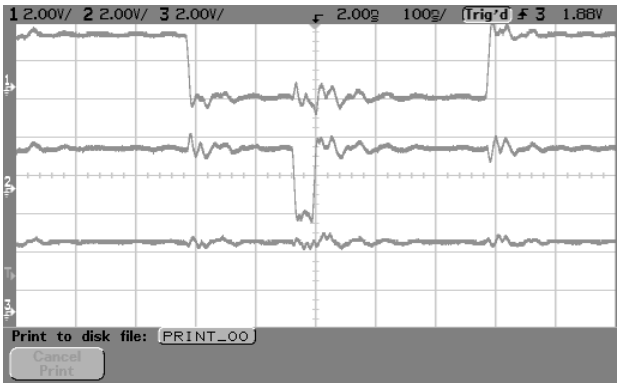


Figure 3.75: Output of the DFT circuitry for the case of fault-free circuit, T_{wt}=40ns. Upper curve: clock signal CK. Middle curve: activation signal ϕ. Lower curve: output signal Q.

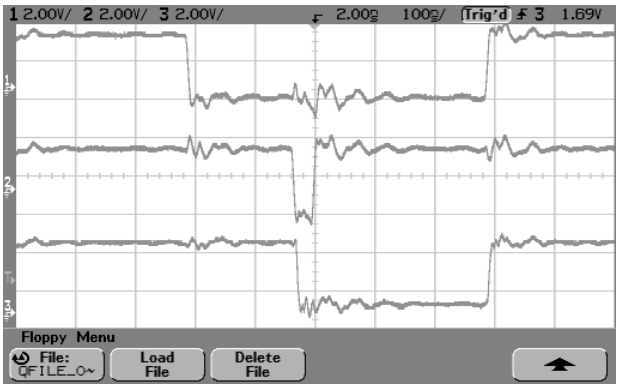


Figure 3.76: Output of the DFT circuitry for the case of R_{open}=∞. Upper curve: clock signal CK. Middle curve: activation signal ϕ. Lower curve: output signal Q.

Finite values of resistive open R_5 can be detected for different pulse width T_{wt} values. The resistive open is simulated with a TG. The voltages at the gates of the TG are V_P=2.02V and V_N=1.1V. Simulation results give R_{open}=38.2KΩ. A width of T_{wt}=260ns is required (See middle panel of Figure 3.77) to detect this open. The output node Q changes to low when ϕ_T=0 (See lower panel of Figure 3.77). Hence, the open is detected. Output node returns to high logic level for the writing phase of the next cycle.

Figure 3.77: Output of the DFT circuitry for the case of R_{open}=38.2KΩ, T_{wt}=260ns. Upper curve: clock signal CK. Middle curve: activation signal ϕ_T. Lower curve: output signal Q.

The minimum required width of the activation signal for different resistive

opens is given in Table 3.13.

t_{wt} (ns)	R_{op} (KΩ)
40	54.3
80	46.9
260	35.8
440	28.7

Table 3.13: Pulse width activation t_{wt} used to detect resistive opens in the clocked inverter stage for the one control signal DFT proposal

3.7.3 Scan path chain

A scan chain composed of three stages have been designed and fabricated. The schematic diagram is given in Figure 3.78.

The detectability of some resistive opens in a scan path chain is analyzed. The proposed chain is shown in Figure 3.78. Each scan cell is composed by a multiplexer and a symmetric flip-flop (See Figure 3.79).

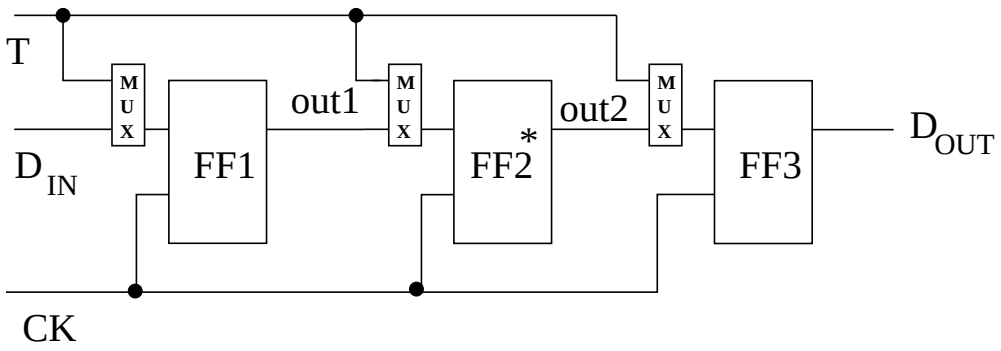


Figure 3.78: Schematic diagram of the scan path circuit.

The analyzed opens are intentionally designed in the second flip-flop (FF2*)

of the scan chain (See Figure 3.78). Two open location have been considered (See Figure 3.79):

- Resistive open R_4 in a conducting path
- Resistive open R_{13} in a multiple open gate

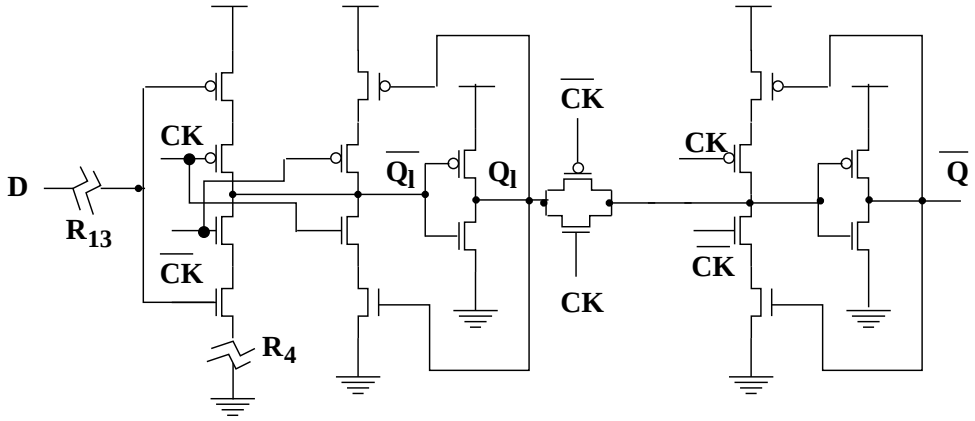


Figure 3.79: The designed opens in the symmetric flip-flop of the scan path chain.

A photograph of the designed and fabricated scan path chain taken with the electronic microscope is shown in Figure 3.80.

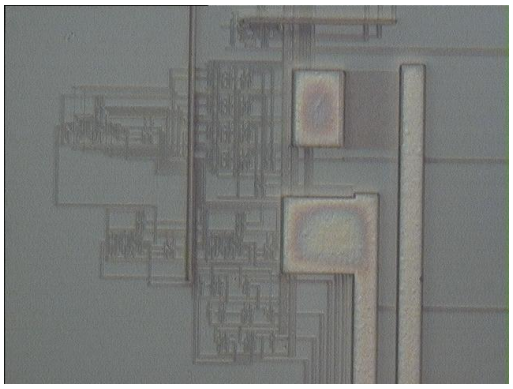


Figure 3.80: Photograph of the fabricated scan path circuit.

The values of resistance of the opens in the experimental measurements have been estimated by simulation with an average estimation of the resistance. The

detectability of the opens was obtained for each clock frequency used during the experimental measurements. In the simulations were used the voltages applied to the gates of the TG of the CUT. First, the voltages at the ends of the transmission gate and the current through it during the charge or discharge through the TG are measured in the simulations.

Then, the average of all the resistance values gives an estimation of the resistance used during the experimental measurements.

The behavior of the scan path chain for low and medium frequencies is shown in Figures 3.81 and 3.82, respectively. The data is changed when the flip-flop is in the writing phase (CK=0 in middle curve of Figure 3.81). Because there are three flip-flops in the scan path chain it is necessary to wait three rising edges to observe an input data change at the output of the scan chain D_{OUT}. Data transitions 0→1 and 1→0 (D_{IN}) are considered (See middle curve).

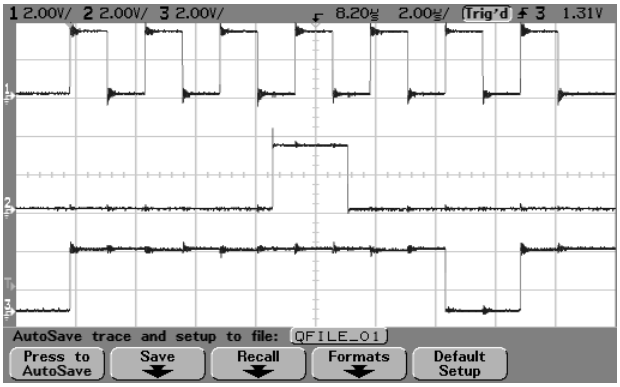


Figure 3.81: Output of the fault-free scan path chain for a clock frequency of 250KHz. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

The voltage at the output node is inverted respect to the input signal because it was not designed the inverter at the output of each flip-flop. This means that for a fault-free case the logic levels at the output D_{OUT} is the complement of the signal at D_{IN}.

Figure 3.82: Output of the scan path for the case of fault-free circuit for 5MHz. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

Resistive open in conducting path

Resistive open R_4 is the analyzed case for open in conducting path (See Figure 3.79). The results are given in Figure 3.83. The resistive open has been fixed to approximately R_4=1.74MΩ. For this resistive open, the used clock period is 200ns (See upper curve in Figure 3.83).

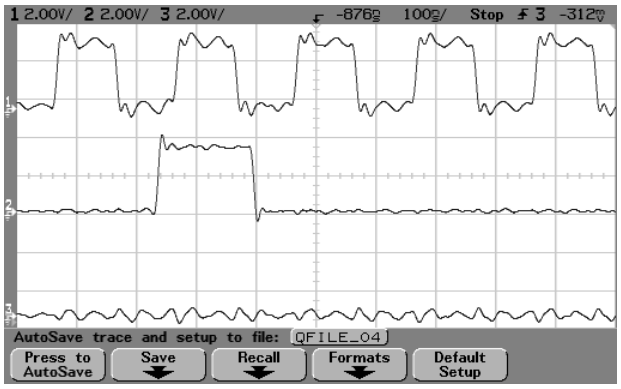


Figure 3.83: Output of the scan path for the case R_4=1.74MΩ and t^*_{xsu}=100ns. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

Input data signal (D_{IN}) is changed for writing phase of the first flip-flop FF1 (See middle curve of Figure 3.83). Data transitions are written and memoryzed for both transitions in the flip-flop FF1 (not shown). However, the faulty flip-

flop FF2* can not write and memoryze data transitions due to the resistive open. Logic error is generated and propagated to the output node of the scan path chain (See lower curve in Figure 3.83) when the clock cycle is made longer than 100ns a correct logic behavior is observed in the scan chain. The critical t^*_{xsu} is 100ns for this open. It should be noted that only half clock cycle is allowed to writing the input data for this open as stated in the previous section.

Different values of t^*_{xsu} are obtained for different values of resistive opens (See Table 3.14). Lower values of t^*_{xsu} are required as the resistive open decreases.

t^*_{xsu} (ns)	R_{op} (KΩ)
100	1740
80	1060
50	570
30	201
10	57

Table 3.14: Measure detectability of the resistive open R_4.

Resistive open in a gate

Resistive open R_{13} has been considered (See Figure 3.79). In this case, it is shown the dependency of the detectability of the open on the initial conditions. It should be noted that the voltage of initial condition is refereed to the right end of the open resistance (See Figure 3.79). A correct logic behavior can be observed in Figure 3.84 for the conditions of the input data applied. The input data is kept constant during 7 clock cycles. The scan output changes three rising edges after the input data changed. This suggests that the intermediate voltage of the initial condition is around $V_{DD}/2$. When the first vector of the input data is kept constant during a lower number of cycles the scan chain fails. It can be observed that the scan output does not change three rising edges after the input data (See Figure 3.85). This is because the intermediate voltage has moved away from the region of $V_{DD}/2$. Because the second vector is also kept constant the scan output

finally changes. In Figure 3.86, it is shown the case where the first vector is kept constant a lower number of cycles than in the previous case. Again, the scan chain fails. The output takes even a longer time to switch to a high logic than in the previous case.

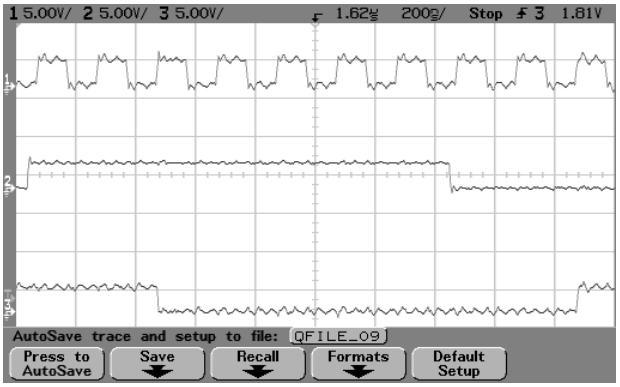


Figure 3.84: Output of the scan path for the case R_{13}=2MΩ. First vector=7 clock cycles. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

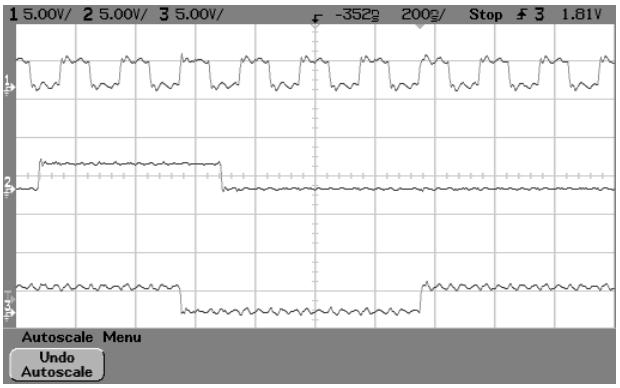


Figure 3.85: Output of the scan path for the case R_{13}=2MΩ. First vector=3 clock cycles. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

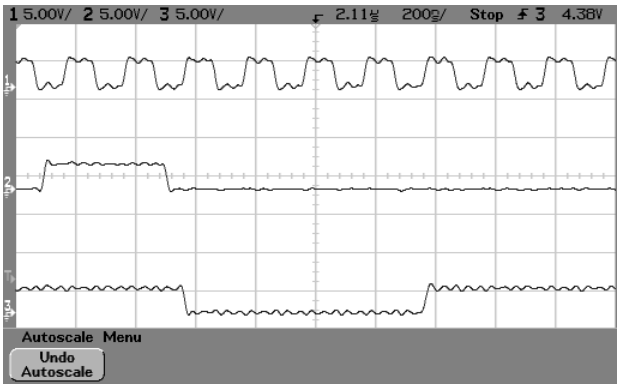


Figure 3.86: Output of the scan path for the case R_{13}=2MΩ. First vector=2 clock cycles. Upper curve: clock signal CK. Middle curve: input signal D_{IN}. Lower curve: output signal D_{OUT}.

3.8 Conclusions

The most important results obtained on this chapter are:

- The behavior and detectability conditions of resistive opens in memory structures has been investigated. Symmetrical and a TG based latches and flip-flops have been considered. However, the results can be extended to other memory structures.

- For opens in the memory elements, except those located in the clocked inverter or closing memory stage, the delay increases as the value of the resistive open increases. Furthermore there is a critical t^*_{xsu} for a logic error to appear in the latch structures. In other words, the optimal detectability conditions should apply the smallest possible time difference between the input data and the leading (memorizing edge) clock edge.

- High resistive opens located in gates, except those located in the clocked inverter or closing memory stage, are dependent on the initial conditions prior to the applications of the two-test vector sequence. The test conditions should observe the output for both applied vectors of the test sequence. This is equivalent to apply both input transitions for this open.

- For high resistive opens located in gates, initial conditions around the middle point of the power supply ($V_{DD}/2$) could not be detected for both input transitions. In this case a short pause time prior to the application of the two-test vector allows that the intermediate voltage goes away from the middle point of the power supply. As a consequence the delay increases and a logic error can appear under certain timing conditions.

- High resistive opens affecting a single gate driven by the clock signal in the driver inverter of the symmetrical latch could be undetected for certain initial conditions. In this case a large pause time could be required for allowing detection of the open. This would increases significantly the test time.

- DFT circuitries have been proposed for opens located in the clocked inverter stage of the symmetrical latch and in the closing memory stage of the TG latch. This allows detection of conducting path opens located in these stages. For the symmetrical lath two proposals are suggested. In the first one, two control signals and two additional transistors are required. In the second one, one control signal and four additional transistors are required. For the TG latch one control signal and one transistor is required. At system level, routing of one control and two control signals is required for the first and second DFT approach, respectively. At global circuit level, the additional inputs can be used for all the memory elements. The power consumption is not significantly affected.

- The detectability of some opens in the TG latch and the flip-flop structures are affected by charge mechanisms. For resistive opens affecting the second inverter in the inverter stage of TG latch, the presence of the TG in the feedback loop of the TG latch allows charge sharing between the input data (after the input stage) and the second inverter in the inverter stage. As a consequence the two-test vector sequence can be invalidated. In this case, charge sharing makes the open more difficult to detect. Charge sharing also appear for resistive open affecting the output inverter in the master latch of the symmetrical flip-flop. In this case, charge sharing makes the open easier to detect. Finally, double charge sharing mechanisms affects opens

in the second inverter of the inverter stage of any latch (master or slave) of the TG flip-flop. For our studied cell, the resulting effect is that the double charge sharing effect can make the open easier or more difficult to detect. This depends on the voltage values before charge sharing to occur.

- Timing conditions for a logic error to appear in a scan path chain have been determined. Three cases have been defined: a) opens after those transistors driven by the clock signal, b) opens before those transistors driven by the clock signal, and c) opens violating the timing conditions of the next fault-free stage. For opens in item a) half clock cycle is allowed to write the data. For opens in item b) a full clock cycle is allowed to write the data. This condition makes an open more difficult to detect. Conditions for opens violating the timing conditions of the next fault-free stage without producing a logic in the defective stage are not easy to find. In general, a non-symmetrical duty clock cycle is required.

- Resistive opens affecting one transistor of the TG gate in the input stage of a latch are hard to detect. These opens are found in the symmetrical and transmission gate latches and flip-flops. In a scan path chain, the difficulty of detection of these opens is even more because a full clock cycle is allowed for writing the input data.

- The two DFT proposals for the symmetrical latch and a scan path chain have been designed and fabricated. AMS 0.35μm CMOS technology has been used. Measurements results show that the two proposed DFT techniques works properly. Opens in a conducting path and in a multiple open gate have been considered in the scan path chain. The measurement results shown the timing dependence of the detectability of these opens. Furthermore, it has also been shown the dependence of opens in gates with the initial conditions.

Chapter 4

Signal X-Y Zoning.

4.1 Introduction

The increasing number of transistors in ICs has made possible faster and more complex circuits. Testing for the signal integrity of these circuits has became also more difficult. Hence, expensive of-chip tester with higher characteristics requirements and high performance capabilities are needed. BIST allows to test some internal nodes difficult to control or to observe at the I/O pins [98] [99]. BIST circuitry is used for controlling and observing directly some nodes of the IC under test. Signal generators and monitoring circuits are included inside the IC.

A BIST proposal has been presented by Brosa and Figueras [100] to detect catastrophic and parametric defects in analog circuits. The number of times that Lissajous curves crossed a control line (dividing the X-Y plane in two) determined the signatures of the defect-free and defective circuits. Control lines were put as lines tangent to the boundaries of defect-free Lissajous curves. A digital binary signature was obtained for each analyzed circuit. The comparison between golden signature (defect-free) and the signature of each case discriminated a defective from a defect-free circuit.

In this chapter, a BIST approach based on surveillancing the inter-signal delays of a class of digital signals by the zones crossed by their X-Y curves is proposed. This method is applied to explore its possibilities to test time critical

applications. Among these we can mention signal integrity violations, clock jitter, transmission line reflections, etc. [101] [102] [103] [104] [89] [105]. Special control lines defining a polygon enclosing the non-defective X-Y curve are employed to separate zones of non-defective from defective signals. Floating gate devices are used to identify defective operating zones. These devices present high dc impedance which means low logic degradation of logic levels of the circuit under test. In analog applications, floating gates devices have used to implement as integrators, low-voltage circuits among others [106] [107] [108] [109].

The rest of this chapter is organized as follows in Section 4.2, the signal X-Y zoning method is presented. In Section 4.3, a BIST circuit implementation to detect delay violations is proposed. In Section 4.4, an application case is illustrated. Finally in Section 4.5, the conclusions of this chapter are given.

4.2 Signal X-Y Zoning Method

In this subsection, first the X-Y zoning curves for critical signals are analyzed. Then, a method based in the X-Y operating zones to detect delay violations of critical signals is explored.

4.2.1 X-Y curves for Inter-Delay Critical Signals

A digital system can be characterized by their input and output signals. Let X and Y be two nodes of a digital system with input vector I(t) applied during the interval [0,T] and S_0 the initial vector state. Let us denote by $X(t)$ and $Y(t)$ the time varying voltages of the signals at nodes X and Y as result of the application of the input waveform $I[0,t]$ when the initial state at time 0 was S_0.

$$X(t) = f_1(t, I[0,t], S_0) \tag{4.1}$$

$$Y(t) = f_2(t, I[0,t], S_0) \tag{4.2}$$

In this chapter, we will center our surveillance on the steady state periodic signals behavior. The method can be extended to take into account the initial state S_0 and the input history $I[0,t]$. In certain circuits such as Phase Locked Loops the transient behavior of the circuit provides additional information. Let's center our attention in steady state periodic digital signals with idealized linear rise and fall transitions. This simplification is not critical and is made for illustrative reasons of the curve shapes.

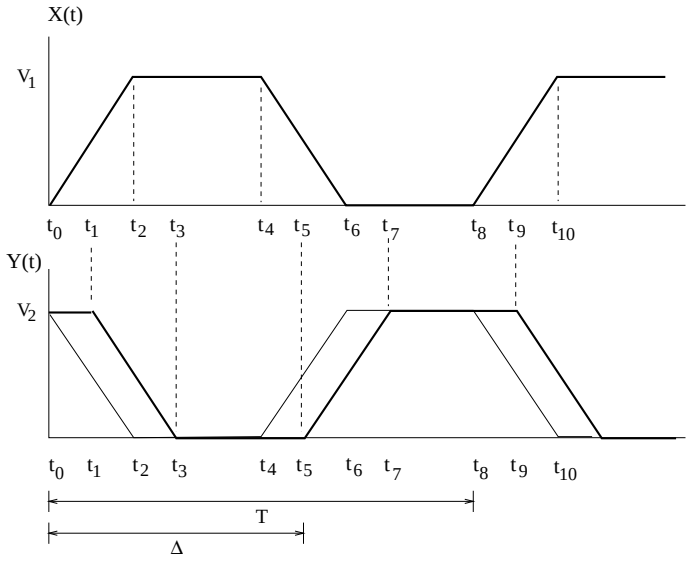


Figure 4.1: Idealized Digital Signals $X(t)$ and $Y(t)$. The signal $Y(t)$ is delayed Δ. In this example, T/2< Δ <3T/4.

In Figure 4.1 idealized digital signals $X(t)$ and $Y(t)$ are shown. The signal $Y(t)$ has a delay Δ with respect to $X(t)$. In this particular example the delay is greater than half period, T/2.

Assume we visualize the voltages $X(t)$ and $Y(t)$ on a oscilloscope in X-Y mode. The curve visualized on the instrument's scope would be the curve obtained eliminating time in expressions 4.1 and 4.2. This curve is the collection of the points:

$$[X(t), Y(t)] \; for \; all \; t \; \epsilon \; [0,t] \tag{4.3}$$

This curve will be called the X-Y curve of the two signal nodes. The concept can be easily extended to N nodes of the circuit. In this case a surface an N dimensional space is obtained.

The X-Y curves for the signals of Figure 4.1 are shown in Figure 4.2. For the non-defective $Y(t)$ signal with T/2 delay with respect to $X(t)$ (i.e. $Y(t)$ is the complement of $X(t)$), the X-Y curve is a straight line with negative slope. However, the X-Y curve changes significantly when the $Y(t)$ signal has suffered a delay increment. In this case the X-Y curve is the external one forming a polygon (See Figure 4.2). The new X-Y curve widens as indicated in Figure 4.2. Each X-Y value represents the relationship of the signals $X(t)$ and $Y(t)$ at different times of their period. These times are indicated as t_0, t_1, t_2, t_3, t_4, t_5, t_6, t_7, t_8 in this illustrative example.

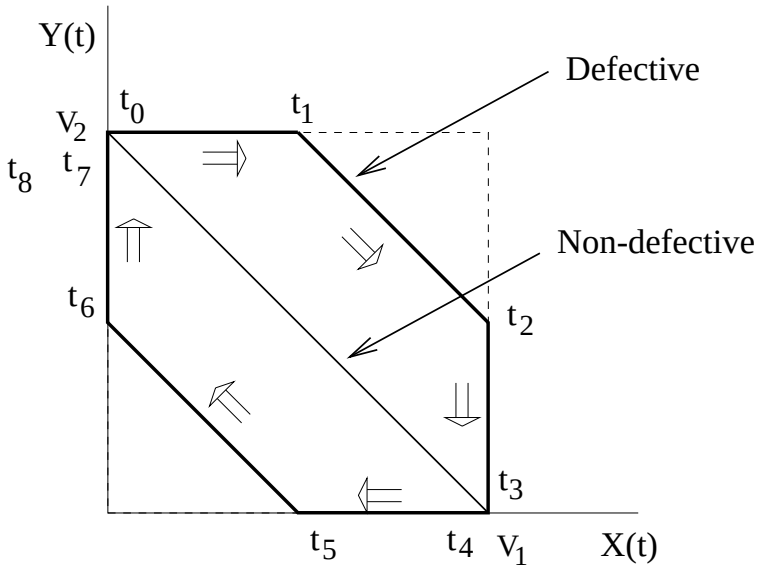


Figure 4.2: X-Y curve of the signals of Figure 4.1. Delay in the interval, T/2< Δ <3T/4.

The X-Y curves for two signals $X(t)$ and $Y(t)$ in phase and for different delay increments are shown in Figure 4.3. The shape of X-Y curves changes depending on the delay increment. For the X-Y curves in phase (Δ=0), the characteristic curve is a straight line with positive slope. A delay between the X-Y curves higher than 0 but lower than T/4 gives as result a characteristic curve similar to an ellipse with positive slope. Delays of Δ=T/4 can be mapped in the X-Y plane

as a circle if enough points are taken into account.Delay between signals $X(t)$ and $Y(t)$ higher than T/4 but lower than T/2 can be mapped as ellipse with negative slope. A straight line with a negative slope is obtained if Δ=T/2. The curves for delays above T/2 (complementary signals) follow a similar pattern. For Δ=T the X-Y curve is obviously the same as for Δ=0 (signals in phase).

4.2.2 Proposed Zoning Method

The signals with zero delay increment and the signals having a delay increment will have different X-Y curves. This property will be used to discriminate the non-defective curve from the defective ones. As the signal $Y(t)$ is delayed from the signal $X(t)$, the shape of the X-Y curve varies (See Figure 4.3). The proposed method is based on the surveillance of the zone of operation of the periodic X-Y curve once the transients have died-out.

In Figure 4.4, it can observed a non-defective X-Y curve enclosed by control lines. The control lines are placed in a way that the non-defective curve never crosses any of the control lines. The control lines define two zones in the X-Y plane: an external zone and an internal zone. Logic values are defined by each zone. A digital 1 is attached to any point of the external zone. A digital 0 is attached to any point of the internal zone. Because this definition, the non-defective X-Y curve (See Figure 4.4) is considered as a digital 0 because the non-defective X-Y curve does not cross the control lines. Defective cases as delay violations give wider X-Y curves than non-defective case (See Figure 4.4) and the control lines are crossed by these cases. Each control line crossing is detected as a transition $0\rightarrow1$ when the X-Y curve evolves from the inside to the outside of the acceptable zone. In a similar way a crossing through the control line is detected as $1\rightarrow0$ transition if the X-Y curve evolves from outside to inside of the acceptable zone.

A *control line* in the X-Y plane is characterized by the following expression:

$$v_z(t) = k_1 X(t) + k_2 Y(t) + k_3 V_n \tag{4.4}$$

where the constants k_1 and k_2 define the slope, and k_3 and V_n define ordinate

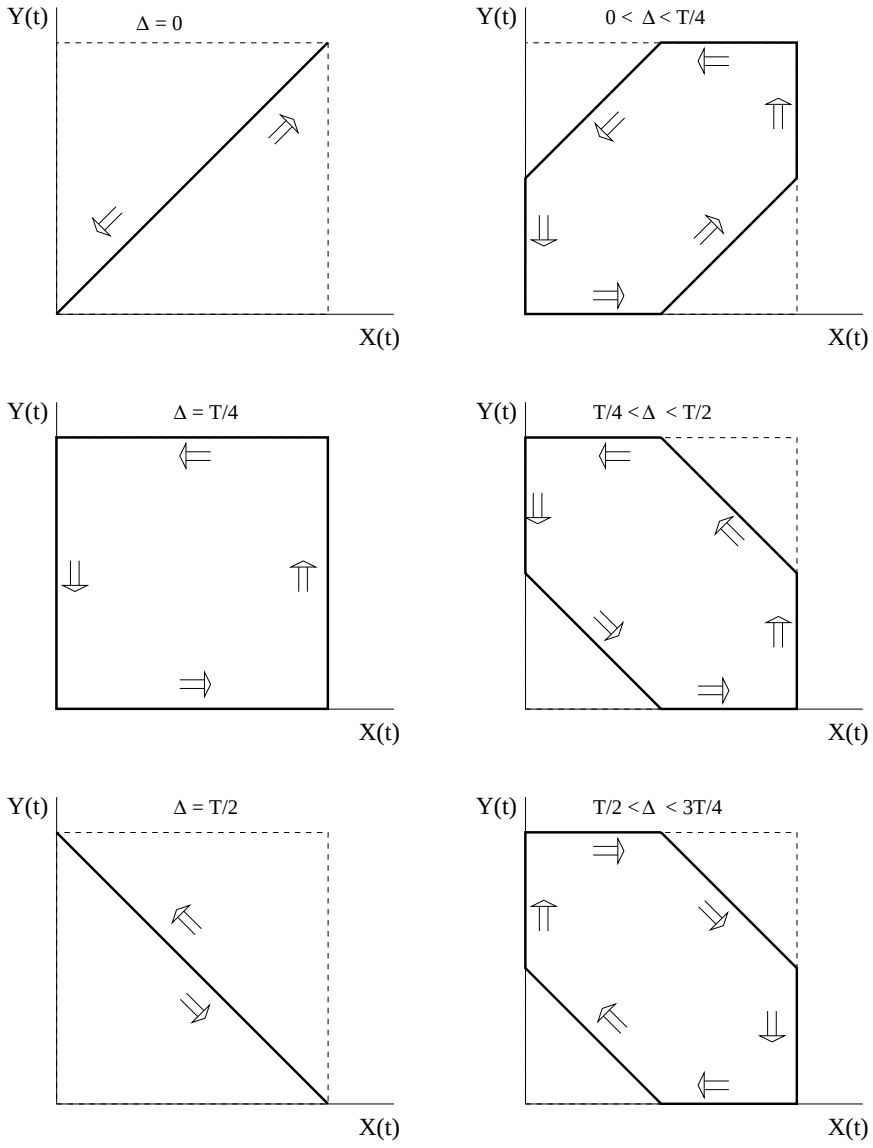


Figure 4.3: X-Y curves of the signals with increasing delay from Δ=0 to T.

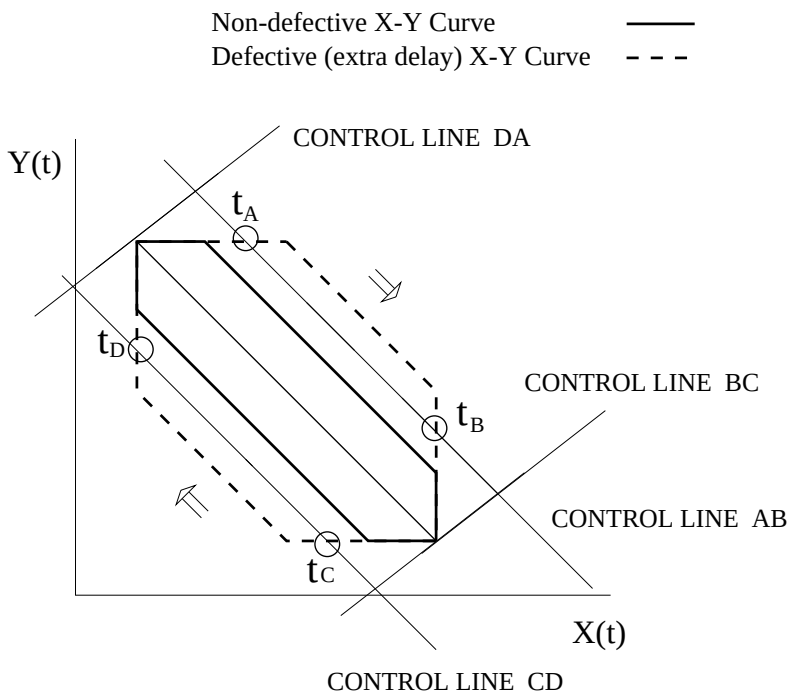


Figure 4.4: X-Y Curves for Non-defective (solid trace) and Delay defective (dotted trace).

at the origin of the control line. This *control line* divides the X-Y plane in two zones: one with $v_z < 0$ and the other with $v_z > 0$. A crossing of one control line with the X-Y curve appears for the condition $v_z = 0$. The result of the crossing points presented in Figure 4.4 are shown in Table 4.1.

In Table 4.1 the crossing of the non-defective and defective curves through each control line are illustrated. The non-defective curve remains always to 0. The defective curve crosses the control lines AB and CD. For these cases, the X-Y defective curve changes from 0 to 1.

This can be easily implemented in a circuitry as will be shown later in the next subsection.

Control Line	Time			
	t_a-t_b	t_b-t_c	t_c-t_d	t_d-t_a
AB	0/1	0/0	0/0	0/0
BC	0/0	0/0	0/0	0/0
CD	0/0	0/0	0/1	0/0
DA	0/0	0/0	0/0	0/0

Table 4.1: Idealized X-Y curves show non-defective / defective values for the curves shown in Figure 4.4.

4.3 BIST Circuit Implementation

In this section an approach of a BIST implementation of the X-Y zoning method is presented. The proposed circuit consists of subzone detectors, an OR gate and a asynchronous counter (See Figure 4.5).

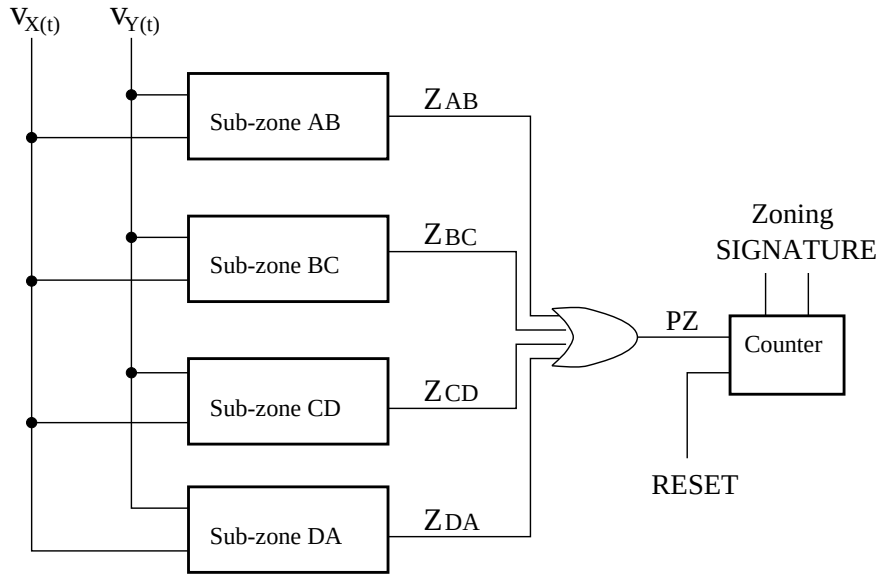


Figure 4.5: Detection circuit block diagram for the X-Y zone verification.

The subzone detector is formed by a X-Y detector and a comparator (See Figure 4.6). The X-Y detector implements the three terms of equation 4.4. The

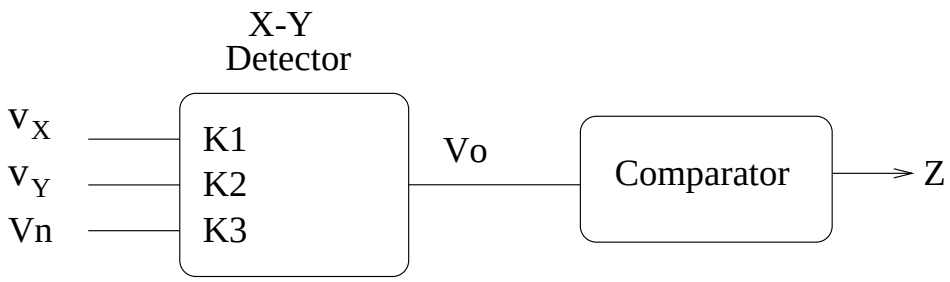


Figure 4.6: Sub-zone detector.

X-Y detector has been implemented with floating transistor gate devices. The comparator gives the condition v_z=0. The OR gate receives signals from each subzone detector. Its output gives information if a X-Y curve is outside of the acceptable zone. The output of the OR gate is connected to an asynchronous digital counter. Ten bits have been used in the application example to be presented in the next subsection. The digital counter will count the transitions given by the OR gate output during a preselectable number of periods. This must be large enough to represent a large digital count (a digital signature) at the counter output for the case of a significative delay variation. Process technology variations as well as environmental changes (P, T, V_{DD}) may produce some extra zone crossings or some may be missed. This will produce some acceptable small changes in the digital signature stored in the counter. The digital signature is given by the state of the asynchronous counter. This is composed by 10 memory devices, the output of these devices define the digital signature [N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0]. The RESET input is used to activate the counting when transients have died-out. The nominal count is given for a preselected number of cycles. In our application example the number of cycles used is 2**9 = 512. For non-defective case, the control lines do not cross the X-Y curve and no digital count is given ([0000000000]). The opposite takes place for defective cases ([0111111111]). In the actual implementation an interval of small values will be considered as non-violating the delay specification whereas a large value in the vicinity of [0111111111] will be an indication of delay violation. Montecarlo simulations as well as worst case analysis will be used in each case to determine the tolerance regions. The difference between the small count (non-defective) compared against a large count (defective) helps to detect delay or signal integrity

violations.

Classical analog weighted adders based in proportional current adding of input signals [110] could be used to implement the X-Y detector. A recent implementation known as floating gate (FG) devices also can be used to implement the weighted adder function [111] [112] [113] [114] of the X-Y detector. The floating gate amplifiers are based in the concept of charge sharing instead of current [115] [116]. These devices allow to carry out the same function that classical adders using fewer elements. Due to their input capacitances, they show a high dc impedance which has low impact in the input signals. Floating transistor gate devices are usually fabricated with two polysilicon levels. The first poly level works as the proper floating gate and the second poly level works as the gate of the transistor. In a standard CMOS digital process floating transistor gate devices can be built using the polysilicon and the metal layers. In Figure 4.7 the schematic of the floating gate transistor is shown.

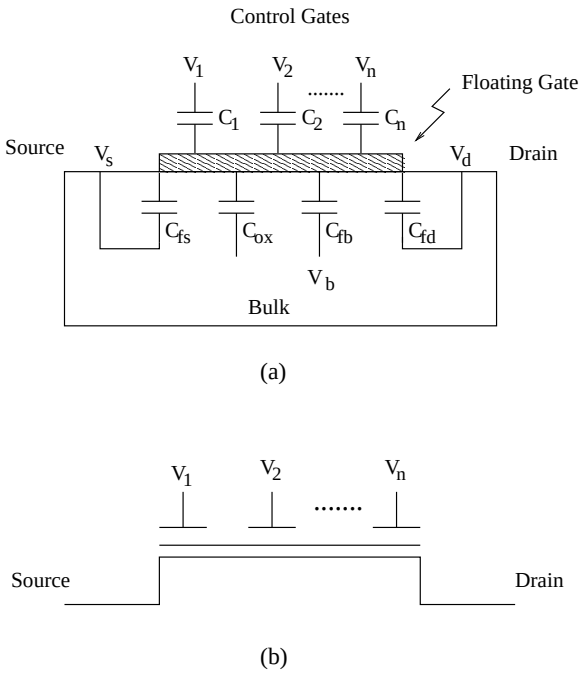


Figure 4.7: Floating gate transistor. a) Circuit model. b) Symbol

C_1 to C_n are the coupling capacitances between poly1 and poly2, V_1 to V_n

are their corresponding control voltages, C_{fd} is the drain to floating gate overlap capacitance, C_{fs} is the source to floating gate overlap capacitance, C_{fb} is the bulk to floating gate overlap capacitance, C_{ox} is the floating gate oxide capacitance. The voltage at the floating node is given by the following expression [115]:

$$V_{floating} = [C_1V_1 + .. + C_nV_n + C_{fs}V_{sb} + C_{fd}V_{db} + C_{ox}\psi + Q_{fg}]\,/C_{sum} \qquad (4.5)$$

where Q_{fg} is the floating gate charge, ψ is the substrate surface potential and C_{sum}=$C_1 + .. + C_n + C_{fs} + C_{fd} + C_{fb} + C_{ox}$.

Floating transistor gate devices are characterized by the weighted gate capacitances that determine their current and threshold voltage [115] [117]. The used detector implemented with floating transistor gate devices at transistor level is shown in Figure 4.8. This topology is used in some high speed comparators. It uses a few elements (differential amplifier plus an amplifier output stage). V_{ref} is the reference voltage. We are exploring other topologies to avoid the use of reference voltage V_{ref}.

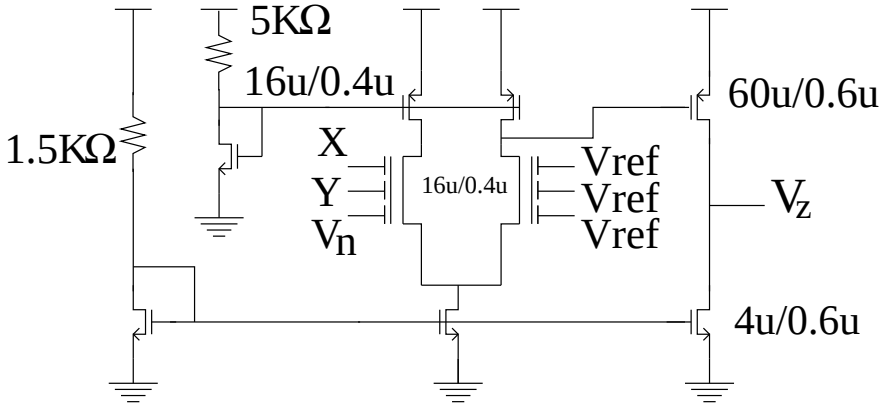


Figure 4.8: Floating gate X-Y detector at transistor level.

The transfer function of this circuit is given by:

$$Vo = A\left[X\frac{C_X}{C_t} + Y\frac{C_Y}{C_t} + V_n\frac{C_n}{C_t} - V_{ref}\right] + \frac{V_{DD}}{2} \qquad (4.6)$$

where A is the detector gain, and X, Y, V_n are the input voltages. C_X, C_Y, C_n are their input capacitances. C_t is the sum of all related capacitances at the floating gate transistor located in the left side (See Figure 4.8).

Comparison between equations defining V_o and (4.4) gives the required parameters to locate the control line in the X-Y plane. Equaling equations 4.4 and 4.6:

$$X\frac{C_X}{C_t} + Y\frac{C_Y}{C_t} + V_n\frac{C_n}{C_t} - V_{ref} = k_1X + k_2Y + k_3v_n \tag{4.7}$$

Hence:

k_1=$\frac{C_X}{C_t}$

k_2=$\frac{C_Y}{C_t}$

k_3=$\frac{C_n}{C_t} - \frac{V_{ref}}{v_n}$

The ratio of the capacitances can be determined by the geometries of the layers used to built the coupling capacitances. The response of this circuit is limited by the time that FG amplifier can detect and amplify the input signals.

4.4 Application Case

In this section, the implemented BIST circuitry is used to test possible delay violation due to crosstalk [118] [63] of capacitive coupled signals.

4.4.1 Crosstalk of Signals

The test vehicle is shown in 4.9. It consists of chains of inverters. Two signals are selected for observation (V_a, V_b) with the X-Y detector circuitry. HP 0.35μm, 4 metal layers, N-well CMOS technology is used. The clock frequency of V_{input} is 500 MHz and the power supply is 3.3V. The routing metal lines are run over the fourth metal level.

The signal sources V_{a1} is a digital continuous trend of pulses. The signal source V_{f1} is complementary to V_{a1} and the signal source of the neighbor line is equal to V_{f1}.

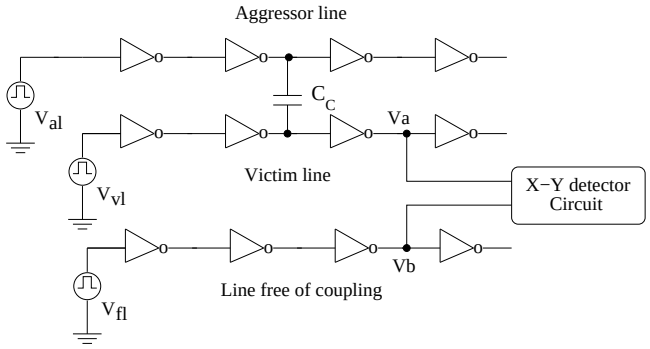


Figure 4.9: Analyzed inverter chain circuit.

The delay can suffer an increment due to the presence of a coupling signal. The delay is larger as the coupling capacitance increases. This fact can be observed in the simulated chronograms of Figure 4.10.

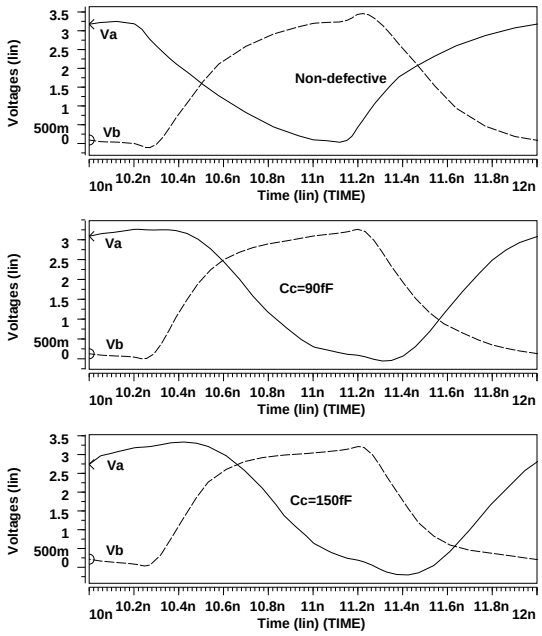


Figure 4.10: Simulated chronograms of the X and Y signals. Top: No coupling. Middle: Capacitive coupling of 90fF. Lower: Capacitive coupling of 150fF.

Larger delays as consequence of crosstalk is detected at the output of the dif-

ferential pair of the floating gate X-Y detector as higher voltage (See Figure 4.11). This voltage is amplified by the output stage of the floating gate X-Y detector.

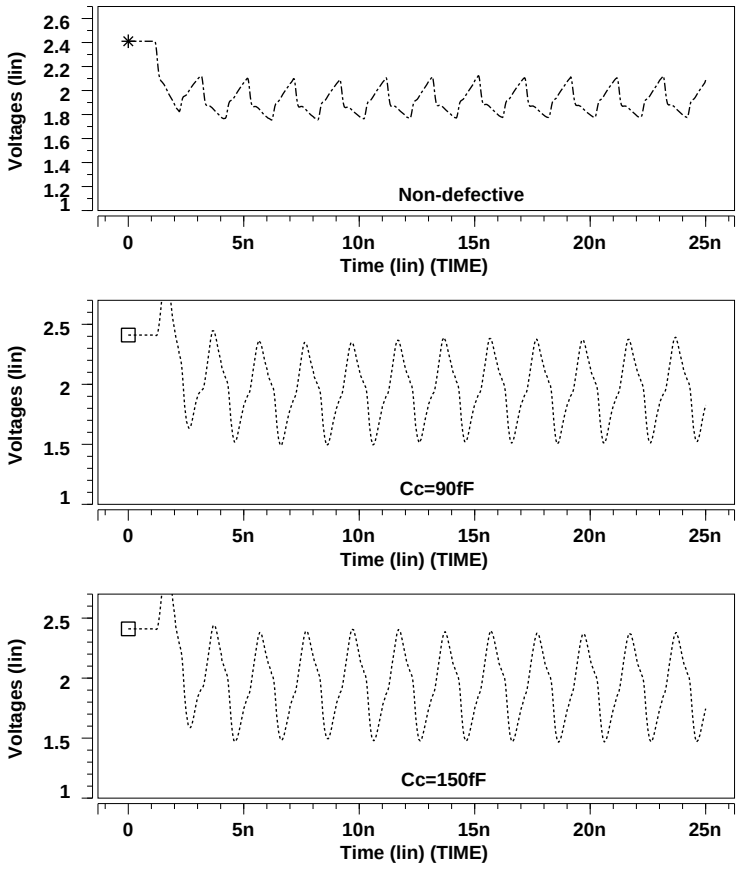


Figure 4.11: Output of the differential pair of the floating gate X-Y detector for fault-free and coupling cases. Top: Without coupling capacitance. Middle: Coupling capacitance = 90fF. Lower: Coupling capacitance = 150fF.

The X-Y operating zones for the circuit shown in Figure 4.9 with and without coupling capacitances are shown in Figure 4.12.

Operating zone curve are given for the following cases: without coupling capacitance effect, C_c=90fF and C_c=150fF. Signals with delay violation have wider X-Y operating zones than for signals with zero delay increment.

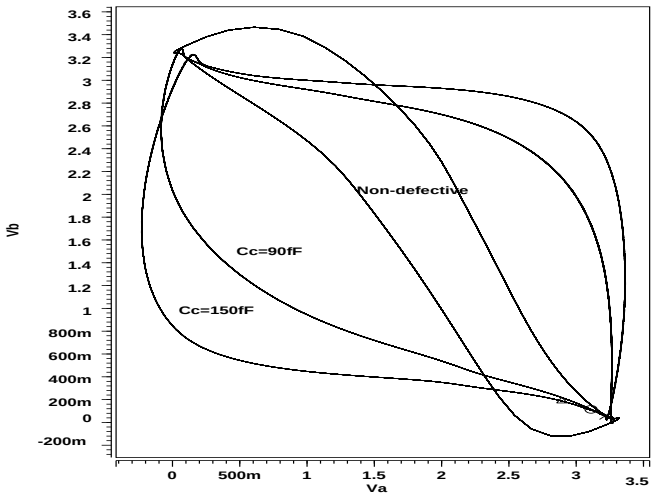


Figure 4.12: X-Y operating zones of defective and non-defective cases. Inverters chain circuit.

4.4.2 Implementation and simulation results

The proposed detector circuit block (See Figure 4.5) has been implemented. The transistor sizes of the X-Y detector are given in Figure 4.8.

The selected control lines are shown in Figure 4.13. Control lines must be selected taking into account process variations. The non-defective region is determined by the control lines 1 and 2 and the lines X=0 volts, V_{DD} and Y=0, V_{DD} (not shown in Figure 4.13). The values of the floating transistor gate capacitances used to fix the control lines are:

- Control line AB: C_X=56fF, C_Y=208fF, C_n=132fF.
- Control line CD: C_X=112fF, C_Y=132fF, C_n=132fF.

Small process and temperature variations cause that X-Y curve is slightly deformed. The displaced non-defective X-Y curve could cross the control lines. This means that a small count deviations at the output of the digital counter can be generated by variations. This can be considered as a non-defective case.

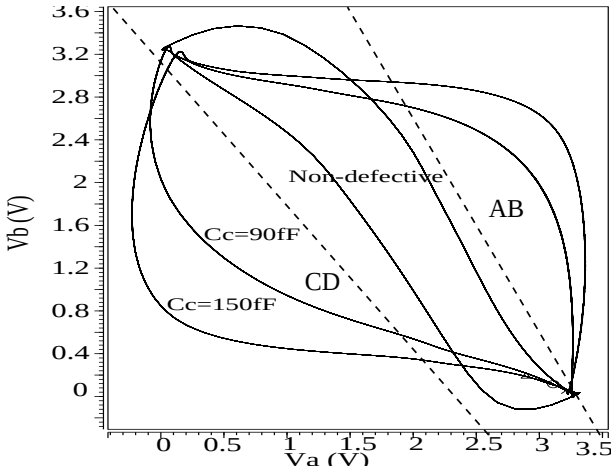


Figure 4.13: X-Y curve non-defective (inner trace). X-Y curves for defective cases (outers traces).

The signals at the OR output (PZ signal in Figure 4.5) for the analyzed cases are shown in Figure 4.14. PZ signal remains at 0 logic level for the case of non-coupling capacitances (See Figure 4.14). For the coupling capacitances cases (C_c=90fF and C_c=150fF) the crossing of the X-Y curve with the control lines are detected as transitions at the OR output (See middle and lower panels of Figure 4.14). The nominal signatures for these cases are:

Nominal signature with no coupling : [0000000000]

Nominal signature with coupling C_c=90fF : [0111111111]

Nominal signature with coupling C_c=150fF : [0111111111]

From these results it can be seen that the delay violation due to crosstalk of signals can be recognized. The obtained signatures have tolerance band because technology and environmental variations can cause additional or missing counts. Due to this, the obtained signature may be different to the nominal signature. It is necessary to establish ranges inside of them to consider the obtained signature as defective or non-defective case. We are currently working on the problem of sizing the tolerance band. Monte Carlo simulations and worse case analysis are expected to provide a systematic way to determine the spread of the signatures

due to technology and environmental variations.

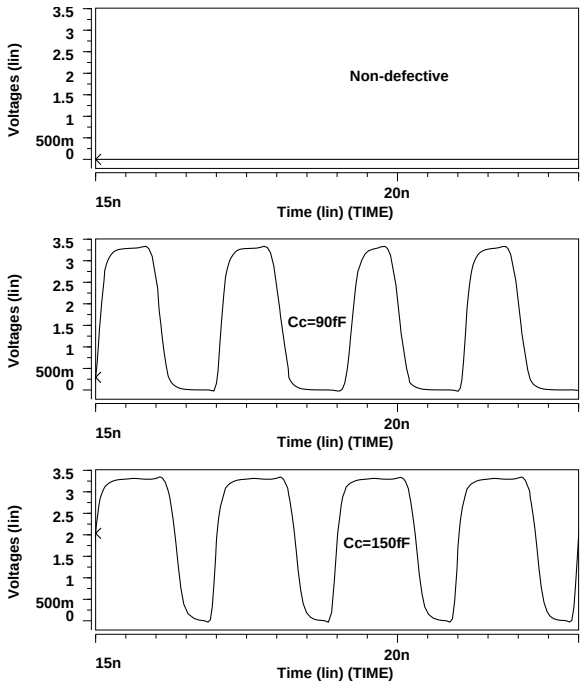


Figure 4.14: Signal at the OR output. Upper panel: non-defective circuit. Middle panel: C_c=90fF. Lower panel: C_c=150fF.

4.5 Conclusions

The most important results for this chapter are:

- A method oriented to detect delay signals violations has been proposed. The used method represents the desired signals in the X-Y plane.
- The X-Y non-defective curve of the circuit is enclosed by control lines. Control lines defines two areas: the inner area and the outer area.
- Defective X-Y curves crosses the area defined by the control lines. Each time that defective curve cross the area of the control lines is detected as a defective case. Control lines can be defined according with its slope and its ordinate at the origin.
- The proposed method can be implemented with subzone detectors. The subzone detectors can be implemented using floating gate devices because its low impact in the circuit under test.
- The method has been applied successfully to detect delay violations due to crosstalk but can be used to other applications.

Chapter 5

Conclusions.

In this thesis, the detectability and test conditions to test open defects have been investigated. Full open defects in combinational circuits and resistive open defects in memory elements have been considered. In addition, a new technique has been proposed to verify time critical digital signals.

The detectability of full interconnection opens by logic and I_{DDQ} testing has been investigated. A coupling capacitive model has been proposed for interconnection opens. This model takes into account technology and topology parameter. Among the important topology parameters we can mention the floating capacitance and the coupling lines affecting the floating one. Explicit analytical expressions for defining the testable regions have been obtained. It has been found that the detectability of these opens is strongly dependent on the signals coupled to the floating one. The values at the coupled signals influences the detectability of the open. For the full controllability case, high coverages of interconnection opens can be obtained using both I_{DDQ} and a stuck-at based test. Furthermore, the relative efficiency of each testing approach also depends on the metal layer affected by the open. It was found that I_{DDQ} testing works better in upper metal layers while a stuck-at based testing works better in lower metal layers. The efficiency of the stuck-at based test decreases for the case of partial controllability. Opens non-detectable by either a stuck-at based or logic testing have been found for the low controllability case. This situation occurs when the most favorable test excitation vectors for a stuck-at based test can not be generated due to the

circuit topology. Routing design for testability techniques should be used in order to make detectable these opens. In addition, the initial trapped charge influences the detectability of the open. The detectable regions changes for the stuck-at based and I_{DDQ} testing techniques depending on the value of the trapped charge. Both techniques should be applied in order to obtain high coverages. Experimental data showing the influence of the defect topology parameters on the behavior of a defective circuit has been presented.

The behavior and exciting conditions of resistive opens in memory structures have been investigated. Two memory structures have been considered: a symmetrical and a transmission gate based. However, the results can be extended to other memory structures.

For opens in the memory elements, except those located in the clocked inverter or closing memory stage, the delay increases as the value of the resistive open increases. Furthermore there is a critical t^*_{xsu} for a logic error to appear in the latch structures. The optimal exciting conditions should apply the smallest possible time difference between the input data and the leading (memorizing edge) clock edge. High resistive opens located in gates, except those located in the clocked inverter or closing memory stage, are dependent on the initial conditions prior to the applications of the two-test vectors sequence. The test conditions should observe the output for both applied vectors of the test sequence. This is equivalent to apply both input transitions. For high resistive opens located in gates, initial conditions around the middle point of the power supply ($V_{DD}/2$) could not be detected for both input transitions. In this case a short pause time prior to the application of the two-test vectors allows that the intermediate voltage goes away from the middle point of the power supply. High resistive opens affecting a single gate driven by the clock signal in the driver inverter of the symmetrical latch could be undetected for certain initial conditions. In this case a large pause time could be required for allowing detection of the open. This would increases significantly the test time.

DFT circuitries have been proposed for opens located in the clocked inverter stage of the symmetrical latch and in the closing memory stage of the TG latch. This allows detection of conducting path opens located in these stages. For the

symmetrical lath two proposals are suggested. In the first one, two control signals and two additional transistors are required. In the second one, one control signal and four additional transistors are required. For the TG latch one control signal and one transistor is required.

The detectability of some opens in the TG latch and both flip-flop structures are affected by charge mechanisms. For some resistive opens in the TG latch, the two-test vector sequence can be invalidated due to charge sharing. In this case, charge sharing makes the open more difficult to detect. Charge sharing in the symmetrical flip-flop makes some opens easier to detect. For opens in a TG flip-flop double charge sharing appears. Charge sharing can make the open easier or more difficult to detect. This depends in voltages prior to charge sharing to occur, Timing conditions for a logic error to appear in a scan path chain have been determined. Three cases have been defined: a) opens after those transistors driven by the clock signal, b) opens before those transistors driven by the clock signal, and c) opens violating the timing conditions of the next fault-free stage. For opens in item a) half clock cycle is allowed to write the data. For opens in item b) a full clock cycle is allowed to write the data. This condition makes an open more difficult to detect. Conditions for opens violating the timing conditions of the next fault-free stage without producing a logic in the defective stage are not easy to find. In general, a non-symmetrical duty clock cycle is required.

The two DFT proposals for the symmetrical latch and a scan path chain have been designed and fabricated. AMS 0.35μm CMOS technology has been used. Measurements results show that the two proposed DFT techniques works properly. Opens in a conducting path and in a multiple open gate have been considered in the scan path chain. The measurement results shown the timing dependence of the detectability of these opens. Furthermore, it has also been shown the dependence of opens in gates with the initial conditions.

In chapter 4, a new BIST technique to verify high speed signals has been presented. A signal X-Y zoning method is proposed to explore the possibilities to test time critical digital signals. The X-Y curve of the analyzed critical signals are enclosed by control lines. Defective X-Y curves are considered when the control lines are crossed by the X-Y curve. A compact and fast BIST circuitry based on

a floating gate weighted adder comparator has been proposed to implement this approach. The X-Y detector implements the control lines defining the operating zones enclosing the X-Y curve of the non-defective signals. The method has been successfully applied to detect delay violations due to crosstalk.

Appendix A

Characteristic MOS Capacitances

The MOS capacitances are divided into two category [119], [120]: the capacitances that belong to the MOS and the interconnect capacitance between two devices. The first one representation is shown in the figure A.1

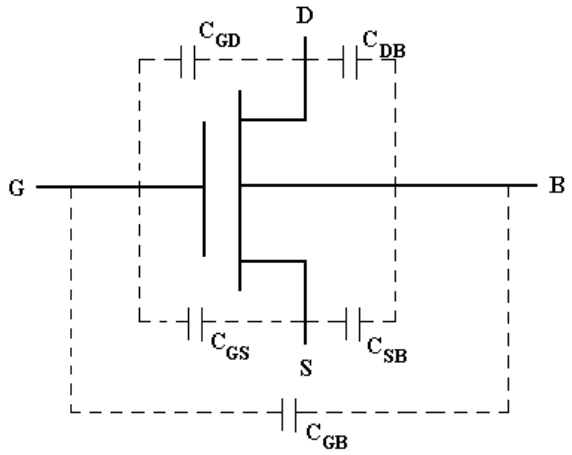


Figure A.1: MOS capacitances.

where C_{gs} is the gate to channel capacitance bound to the source region, C_{gd} is the gate to channel capacitance bound to the drainage region, C_{sb} is the source-diffusion to substrate capacitance, C_{db} is the drainage-diffusion to substrate capacitance, C_{gb} is the gate to substrate capacitance.

The total gate capacitance of a MOS transistor is

$$C_g = C_{gb} + C_{gs} + C_{gd} \tag{A.1}$$

The own capacitances of the MOS are divided into gate capacitances and diffusion capacitances. The capacitances showed by a MOS device are not constant when the polarization conditions are changing. The gate capacitances of a MOS according with the gate voltage are the next:

1.- Cut off region ($V_{gs} < V_t$): In this region the MOS remains in the region of cut-off, then will be not channel and $C_{gs} = C_{gd} = 0$ is taken. Usually the MOS device is modeled as a serial combination of :

$$C_{dep} = \frac{\varepsilon_o \varepsilon_{si}}{d} A \tag{A.2}$$

$$C_o = \frac{\varepsilon_{sio_2} \varepsilon_o}{t_{ox}} A \tag{A.3}$$

where A is the area of the gate, ε_{sio_2} is a dielectric constant, ε_{si} is the silice constant dielectric, ε_o is the free space permitivity, d is the depth of the desertion region.

2.- Not saturate region ($V_{gs} - V_t > V_{ds}$): At this point the channel is well formed and C_{gs} y C_{gd} capacitances are important now

$$C_{gd} = C_{gs} = \frac{1}{2} \frac{\varepsilon_{Sio_2} \varepsilon_o}{t_{ox}} A \tag{A.4}$$

and C_{gd} is zero

3.- Saturate region ($V_{gs} - V_t < V_{ds}$): Here the channel is in strong inversion, so C_{gd}=0 and gate to source capacitance is (C_{gs}):

$$C_{gs} = \frac{2}{3} \frac{\varepsilon_{Sio_2} \varepsilon_o}{t_{ox}} A \tag{A.5}$$

The next step is to know the diffusion capacitances, all the diffusion regions have an associate capacitance to substrate which depends on the voltage between the diffusion region and the substrate. These are subdivided into:

- Channel to substrate joint capacitance C_{bc}
- Source to substrate joint capacitance C_{jsb}
- Drain to substrate joint capacitance C_{jdb}

Channel to substrate joint capacitance is given by:

$$C_{bc} = WLC_j \tag{A.6}$$

$$C_j = \frac{\varepsilon_{Si}}{t_{si}} \tag{A.7}$$

where t_{si} is the desertion region depth between the channel and the substrate, this depth depends on the region desertion voltage V_{bc} and the substrate doped level N_{sub}

$$t_{si} = \sqrt{\frac{2\varepsilon_{si}(\phi_j - V_{bc})}{qN_{sub}}} \tag{A.8}$$

where V_{bc} is the channel to substrate potential, which normally is taken as $V_{bc} = V_{bs}$, ϕ_j is the interbuild joint to substrate voltage

$$\phi_j = \frac{KT}{q} ln \frac{N_c N_{sub}}{ni^2} \tag{A.9}$$

Joint to drainage and joint to source capacitances are to build by two components, they are perimeter and area joint capacitances

$$C_{jsb} = A_s C_{sb} + P_s C_{swsb} \tag{A.10}$$

$$C_{jdb} = A_d C_{db} + P_d C_{swdb} \tag{A.11}$$

where P_s is the source perimeter, P_d is the drain perimeter, A_s is the source area, A_d is the drain area.

$$C_{sb} = \frac{C_j}{(1 - \frac{V_{bs}}{\phi_j})^{0.5}} \tag{A.12}$$

$$C_{swbs} = \frac{C_{sw}}{(1 - \frac{V_{bs}}{\phi_j})^{0.5}} \tag{A.13}$$

$$C_{bd} = \frac{C_j}{(1 - \frac{V_{bd}}{\phi_j})^{0.5}} \tag{A.14}$$

$$C_{swbd} = \frac{C_{sw}}{(1 - \frac{V_{bd}}{\phi_j})^{0.5}} \tag{A.15}$$

The next table summarizes the MOS capacitances according with the operation region, it is important to take into account the expressions given before

V_{ent}	P	N	P	N
$0V_{dd}$	C_{bd}	C_{bd}	C_{ox}	$C_{ox} + \frac{2}{3}C_{gs}$
$\frac{1}{2}V_{dd}$	$C_{bd} + \frac{1}{2}C_{gd}$	$C_{bd} + \frac{1}{2}C_{gd}$	$C_{ox} + \frac{1}{2}C_{gs} + \frac{1}{2}C_{gd}$	$C_{ox} + \frac{1}{2}C_{gs} + \frac{1}{2}C_{gd}$
V_{dd}	C_{bd}	C_{bd}	$C_{ox} + \frac{2}{3}C_{gs}$	C_{ox}

Table A.1: MOS capacitances.

Appendix B

Floating Gate Devices

The floating gate devices are based in the weighted summation. This operation is realized by Kirchoff's current law.

$$Y_i = \sum_{i=1}^{n} W_i X_i$$

where Y_i is the output, W_i are the weights, X_i are the input. There are two ways of implement weighted summation: adding current in a node through voltage controlled current source or sharing charge through coupling capacitors. The coupling capacitor method was introduced by [111]. The model is resolved by conservation of charge in the floating node. The input voltages are kept constant. A system with floating capacitances is based in the idea of charge sharing instead of current sum. This kind of devices uses a weighted sum capacitance at the gate input to determine the threshold voltage and the current through device. Floating capacitors can be matched better than transistors, they are easily implemented, they have very small parasitic capacitance. Methods to modeling floating gate to avoid convergence problems can be found in [121].

The floating gate MOS devices or neuron MOS ([111], [114], [121], [115], [117]) are usually make with two polysilicon levels. The first polysilicon layer is the floating transistor gate and the second one is the proper gate of the transistor. In figure B.1 the floating gate MOS can be seen . Figure a) shows the capacitor model and b) is the symbol.

C_1 to C_n are the coupling capacitances between poly1 and poly2, V_1 to V_n are

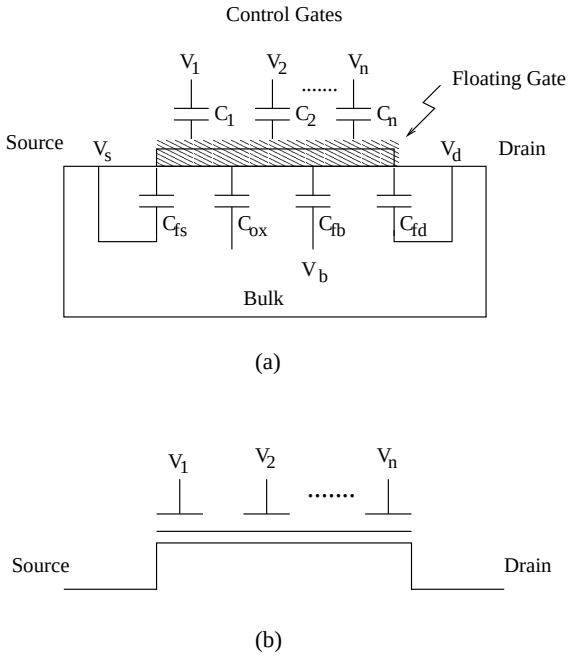


Figure B.1: Floating gate MOS. a) Capacitor model. b) Symbol circuit.

their corresponding voltages, C_{fd} is the drain to floating gate overlap capacitance, C_{fs} is the source to floating gate overlap capacitance, C_{fb} is the bulk to floating gate overlap capacitance, C_{ox} is the floating gate oxide capacitance. Between its characteristics [121] are the charge retention inyected in the floating gate and the sum operation of linear weighted voltage utilizing a capacitive coupling effect. The voltage at the floating node is determined by the charge in the floating gate which can be expressed in the next form [115]:

$$V_{floating} = [C_1V_1 + C_2V_2 + ... + C_nV_n + C_{fs}V_{sb} + C_{fd}V_{db} + C_{ox}\psi + Q_{fg}]/C_{sum} \tag{B.1}$$

where Q_{fg} is the floating gate charge after fabrication and usually is not zero, ψ is the susbtrate surface potential and $C_{sum} = C_1+....+C_n+C_{fs}+C_{fd}+C_{fb}+C_{ox}$. Moduling the voltage at the floating gate by the coupling capacitances made possible to controlling the drain current and the operation point. This is the special characteristic of floating gate devices. Floating gate CMOS transistors can operate in a similar way that conventional CMOS transistors: subthreshold and above threshold.

Subthreshold

For this region the control gate voltage controls the surface potential as a function quasi-linear. Drain to source current in floating gate devices is given by the next:

$$I_D = \frac{W}{L} I_o e^{\frac{\zeta_C (V_1 + \ldots + V_n)}{U_t}} e^{\frac{\zeta_B V_{sb} + \zeta_D V_{db}}{U_t}} (e^{\frac{-V_{sb}}{U_t}} - e^{\frac{-V_{db}}{U_t}}) \tag{B.2}$$

where W is the channel width, L is the channel length, I_o is the current factor, $\zeta_C \equiv k\frac{C_{fc}}{C^*_{sum}}$, $\zeta_S \equiv k\frac{C_{fs}}{C^*_{sum}}$, $\zeta_D \equiv k\frac{C_{fd}}{C^*_{sum}}$, C^*_{sum}=$C_{sum} - kC_{ox}$, k is the gate efficiency, U_t is the thermal voltage. The transconductance in saturation region ($V_{DS} > 4U_t$) is given by:

$$g_m = \frac{\zeta_C I_D}{U_t} \tag{B.3}$$

The output conductance is given by the next:

$$g^*_d = g_d + \frac{\zeta_D I_D}{U_t} \tag{B.4}$$

$$g_d \simeq \frac{I_{DS}}{V_o}$$

V_o is similar to the Early voltage is experimentally determined.

Above Subthreshold

For region above subthreshold the surface potential does not depend on the gate voltage. It remains near $2\phi_F + V_{sb}$. In the linear region, the current in the channel is given by:

$$I_D = K|F(V_{floating}, V_{sb} - F(V_{floating}, V_{db})) \tag{B.5}$$

where $F(V_{floating}, V) = (V_{floating} - V_{TH} - V)^2 + \frac{4}{3}\gamma(V + 2\phi_F)^{\frac{3}{2}}$, $K = \frac{W\mu\epsilon_{ox}}{2Lt_{ox}}$, $\gamma = \frac{t_{ox}}{\epsilon_{ox}}\sqrt{2q\epsilon_{ox}N_B}$, V_{TH} is the threshold voltage, N_B is the substrate doping

concentration, t_{ox} is the gate oxide thickness. In saturation the current in the channel is given by:

$$I_D = KF(V_{floating}, V_{sb}) \tag{B.6}$$

The transconductance is the next:

$$g_m = \frac{2C_{fo}\sqrt{KI_D}}{C_{sum}} \tag{B.7}$$

The output conductance is as next:

$$g_d^* = g_d + \frac{2C_{fd}\sqrt{KI_D}}{C_{sum}} \tag{B.8}$$

The general transfer characteristic for a floating gate CMOS is the same in any operation region $i = g_m(V_1 + V_2 + ... + V_n)$.

Resumen

El campo de la electrónica ha estado cimentado en el transistor de silicio desde los años ochentas. Transistores cada vez mas pequeños han sido posibles debido al avance de la electrónica en la litografía y los procesos de fabricación. Como consecuencia se ha incrementado la densidad de integración y la complejidad de los circuitos integrados. Sin embargo varios tipos de defectos pueden aparecer debido a las alteraciones en los procesos de fabricación los cuales pueden afectar a la funcionabilidad de los circuitos integrados (CI). Los defectos se pueden clasificar de acuerdo a su impacto como paramétricos y catastróficos. El impacto de los defectos paramétricos puede ser global lo cual afecta a todo el CI o bien local el cual afecta a solo una area del CI. Existe un amplia gama de causas que provocan los defectos paramétricos entre las cuales se puede mencionar a las siguientes: variaciones del gradiente de temperatura durante el proceso de grabado, aberraciones locales de los lentes, variaciones del proceso de dopado.
Los defectos catastróficos afectan a la funcionabilidad de los CI como fallos permanentes, intermitentes o transitorios. Los fallos permanentes pueden ser el resultado de corto circuitos, abiertos, cortos en el oxido de compuerta y otros defectos. Los fallos intermitentes son aquellos que son excitados por una probabilidad no cero. Los fallos transitorios son debidos a eventos transitorios como partículas alfa o fenómenos de ruido como acoplamiento capacitivo o variaciones en las líneas de tierra o alimentación.

El trabajo de esta tesis se enfoca principalmente a defectos de abiertos. Se consideran abiertos totales y abiertos parciales (abiertos resistivos). Un abierto total es aquel en el cual no existe influencia de la señal de entrada sobre la línea flotante. Un abierto resistivo es aquel en el cual el material conductor no esta

completamente roto por lo cual la resistencia de la línea se ve incrementada. Los puntos probables en los cuales puede tener lugar un abierto total o un abierto resistivo son los puntos de interconexión entre metales (vías) o los puntos de interconexión entre area activa y metal/polisilicio (contactos). Un contacto o vía mal formada da como resultado una conexión defectuosa. Sin embargo estas no son las únicas causas de abiertos, también podemos mencionar a las siguientes causas:

- Humedad residual en la vía después del grabado.
- Insuficiente llenado de la vía.
- Desalineamiento de la vía que afecta su conectividad y su tamaño.
- Deposito de aluminio a alta temperatura.
- Microfracturas en el proceso del óxido.
- Electromigración.

La finalidad de las pruebas es detectar los fallos con el fin de identificar a los circuitos que no cumplan con las especificaciones. Por lo que una secuencia de prueba se puede dividir en los siguientes pasos:

- Aplique vectores de entrada en las entradas controlables del circuito.
- Mida la salida en una salida observable.
- Compare el valor medido contra un valor de referencia para determinar si el circuito se acepta o rechaza.

Un fallo se puede representar a diferentes niveles de abstracción como nivel eléctrico, lógico o funcional. Entre los modelos mas ampliamente usados esta el modelo stuck-at, el modelo stuck-open, el modelo stuck-on, el modelo de corto.
Un fallo se puede detectar usando diferentes tipos de pruebas, entre las más comunes se encuentran las siguientes:
Prueba lógica la cual monitorea los niveles lógicos de los circuitos bajo prueba, **prueba de corriente** la cual monitorea el nivel de corriente de la fuente de alimentación del circuito bajo prueba, **prueba de retardo** la cual observa las

condiciones de sincronización del circuito bajo prueba.

Un abierto total desconecta el camino de conducción de una compuerta manejadora de una compuerta manejada. Debido al abierto los transistores Pmos y Nmos de la compuerta manejada flotan. Este tipo de fallos tiene la mayor probabilidad de ocurrencia y un lugar muy probable son las vías. En este trabajo se presenta un modelo eléctrico para un abierto de interconexión. El cual ha sido dividido de acuerdo a su topología y una expresión analítica la cual predice el voltaje en el nodo flotante es obtenida. La detectabilidad de este tipo de abiertos puede ser asegurada por medio de pruebas lógica y de corriente, para tal efecto es posible obtener diferentes condiciones de prueba para cuatro posibles situaciones:

- Controlabilidad total
- Controlabilidad parcial
- Carga inicial atrapada
- Baja controlabilidad

Para el caso de **controlabilidad total** todos los posibles vectores de excitación pueden ser generados.

V_i	$V_{ci}...V_{cn}$	Detectable range V_{if}	Fault
0	0	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
0	1	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
1	0	$[0, V_{TN}]$	SA-0
1	1	$[0, V_{TN}]$	SA-0

Esto significa que es posible detectar un abierto como un stuck-at 1 si voltaje en el nodo flotante es cuando menos $V_{DD} - |V_{TP}|$ para un voltaje de acoplo alto o bajo y un voltaje de la compuerta manejadora bajo. El abierto también puede ser detectado como un stuck-at 0 si el voltaje en la compuerta flotante es cuando mas V_{TN} para un voltaje de acoplo alto o bajo y un voltaje de la compuerta manejadora alto.

La detectabilidad de los abiertos puede ser garantizada por medio de detectada por medio de una prueba de corriente si el voltaje en el nodo flotante permanece entre V_{TN} y $V_{DD} - |V_{TP}|$.
Entonces considerando los voltajes de la líneas de acoplo y los voltajes que se pueden alcanzar en el nodo flotante se puede garantizar la detectabilidad del circuito para las siguientes condiciones:

- V_{TN} con C_c a V_{DD}
- $V_{DD} - |V_{TP}|$ con C_c a V_{DD}
- V_{TN} con C_c a V_{GND}
- $V_{DD} - |V_{TP}|$ con C_c a V_{GND}

Se han obtenido expresiones analíticas para las cuatro condiciones previas de detectabilidad donde una combinación de una prueba lógica y una prueba de corriente detecta a la mayoría de los abiertos. Sin embargo para casos extremos de grandes ruteados, pequeños acoplos y de pequeños ruteados, grandes acoplos una prueba lógica puede ser suficiente para garantizar la detectabilidad de un abierto. En el caso de acoplos y ruteados medios es posible que con solo una prueba de corriente se detecte el abierto.
Para el caso de **controlabilidad parcial** las señales de acoplo no pueden ser controladas simultáneamente a 1 o 0 por lo que las condiciones mas favorables para probar los abiertos no pueden ser generadas. La detectabilidad del mapa de pruebas obtenido por medio de las condiciones analíticas del caso de controlabilidad total se ve significativamente reducido a dos regiones separadas de prueba lógica y prueba de corriente.
En el caso de **carga inicial atrapada** se toma una variación de esta en un rango de [-0.3V, +0.3V] de acuerdo a lo mencionado en la literatura para el caso de controlabilidad total considerando que todo el ruteado se encuentra sobre el sustrato. El resultado es que las regiones de detectabilidad obtenidas para el caso de controlabilidad total incrementan su rango permitiendo la aparición de zonas las cuales no se pueden asegurar si son detectables por medio de prueba lógica o de corriente.
En el caso de **baja controlabilidad** puede ser que las condiciones de prueba

más favorables no puedan ser generadas y de manera similar al caso de controlabilidad parcial algunas regiones de detectabilidad no aparezcan. Sin embargo técnicas de ruteo pueden ser empleadas para hacer detectables aquellos casos no detectables por prueba lógica o prueba de corriente. La técnica empleada separa físicamente las líneas adyacentes involucradas. Las líneas son separadas hasta que son detectables por prueba lógica o prueba de corriente. Otra técnica alternativa consiste en colocar una línea de blindaje entre la línea bajo prueba y la línea adyacente acoplada.

Como parte de abiertos totales, también se analizo el caso de abiertos totales en compuertas no sensibilizadas. De manera general un sistema digital puede no solo tener compuertas sensibilizadas si no que también compuertas no sensibilizadas por lo que la respuesta de un sistema de este tipo es determinada por la suma de un sistema sensibilizado mas un sistema no sensibilizado. En general en un sistema no sensibilizado los voltajes en el drenaje y fuente de un transistor pueden no tener niveles lógicos bien definidos por lo que una expresión analítica en el nodo flotante también será función de los voltajes de drenaje y fuente. Las condiciones de detectabilidad pueden ser resumidas en cuatro expresiones de manera semejante al caso de compuertas sensibilizadas. Sin embargo los casos de análisis no se reduce a cuatro casos si no que un total de 16 casos cubren el espectro total de combinaciones posibles de voltajes en el drenaje y fuente. Como resultado se observa un amplio rango de variación en cada región de detectabilidad a medida que el numero de compuertas no sensibilizadas aumenta, esto significa que pueden aparecer rangos de defectos que no son detectables.

En conclusión en el tema de abiertos totales se investigo la detectabilidad de los abiertos de interconexiones por medio de prueba lógica y de corriente. Por medio de un modelo se tomaron en cuenta factores como la tecnología y parámetros topologicos (capacitancias de ruteo y de acoplo) que fueron plasmados en expresiones analíticas. También se encontró que pruebas basadas en modelos stuck-at funcionan mejor para bajos niveles de metal mientras que pruebas basadas en corriente son mas adecuadas para los altos niveles de metal. De acuerdo a como la controlabilidad de un caso disminuye, la eficiencia de la prueba

por medio del modelo stuck-at también disminuye o bien pueden no ser detectables por prueba lógica o de corriente. Debido a las compuertas no sensibilizadas puede aparecer un rango de defectos que no son detectables por medio de prueba lógica o prueba de corriente.

Sin embargo el analísis no solo se limitó al caso de abiertos totales si no que también al caso de abiertos resistivos. Se analizarón las siguientes estructuras de memoria: **latch simétrico**, **latch de compuertas de transmisión**, **flip-flop simétrico**, **flip-flop de compuertas de transmisión**, **cadena scan path**. El analísis se ha hecho para diferentes localizaciones probables de abiertos resistivos. Para los casos de abiertos resistivos indetectables, se ha utilizado una técnica de DFT con el fin de hacerlos detectables. También se ha analizado los casos en donde se presenta el efecto de redistribución de carga.
En el caso del **latch simétrico** la detectabilidad de los abiertos resistivos se lleva a cabo por medio de la utilización de una secuencia de dos vectores, en donde el primer vector se utiliza para inicializar el latch a 0 o 1, y el segundo vector es utilizado para conmutar hacia el estado complementario. Después de un cierto tiempo es observada la salida. Si la respuesta del latch es la misma que la esperada entonces el latch esta libre de fallos de otra forma esta defectuoso. También se analiza el efecto de la condición inicial anterior a la aplicación de la secuencia de los dos vectores. El comportamiento de los casos de abiertos resistivos se observa por medio del parámetro t_{xsu}, el cual es el tiempo desde que el segundo vector cambia hasta que la llegada del flanco de memoria del reloj.

El analísis en el latch simétrico se hace de acuerdo a las etapas en las que esta compuesto: manejadora (abiertos resistivos en el camino de conducción y abiertos resistivos en compuertas), inversora manejada por reloj (abiertos resistivos en el camino de conducción, abiertos resistivos en el camino de control, abiertos resistivos en el camino de retroalimentación) y de salida (abiertos resistivos en el camino de conducción y abiertos resistivos en compuertas). Los casos en la etapa manejadora y de salida presentan un comportamiento muy similar, abiertos resistivos en el camino de conducción son detectados para valores suficientemente largos de t_{xsu} utilizando solo una transición del dato de entrada. Para el caso de abiertos resistivos en compuertas, puede ser que estas sean múltiple o simples, en

múltiples compuertas cualquier vector de entrada 0→1 o 1→0 puede ser aplicado para excitar a este caso. Si el caso analizado tiene un valor alto de resistencia, entonces el tiempo de respuesta del latch puede depender del voltaje de condiciones iniciales en el fallo, pero si el voltaje inicial se encuentra en las proximidades de $V_{DD}/2$, entonces puede que no sea detectado. Para el caso de un simple abierto de compuerta entonces solo un vector de entrada podrá ser aplicable.

Los abiertos resistivos localizados en la etapa inversora manejada por reloj son tradicionalmente indetectables. Los abiertos resistivos en el camino de retroalimentación no son detectables por medio de prueba lógica o por medio de prueba de retardo, sin embargo su comportamiento para grandes abiertos resistivos depende del voltaje de condición inicial y pueden ser detectados por medio de una prueba de retención de datos. En el caso de abiertos en el camino de conducción tampoco es posible detectarlos por medio de pruebas lógicas o de retardo, sin embargo una prueba de retención de datos podría detectarles. Para este caso se recomienda que se utilizen técnicas de layout para reducir la probabilidad de ocurrencia de estos abiertos. Los abiertos resistivos en el camino de conducción muestran que para grandes fallos una prueba de retención de datos puede ser suficiente para detectalos. Sin embargo con el fin de incrementar el rango de detectabilidad, se proponen dos técnicas de DFT: con una señal de control, con dos señales de control. La propuesta de dos señales de control requiere de dos transistores (un Pmos y un Nmos) y dos señales de control adicionales. El transistor DFT Pmos se activa para detectar abiertos resistivos en la red Nmos y viceversa. La competencia entre la red Nmos y el transistor DFT Pmos determina si el camino de conducción presenta fallos o no. La propuesta de una señal utiliza cuatro transistores adicionales (un Nmos, un Pmos y un inversor) y una sola señal de control. Los transistores DFT (Nmos, Pmos) se activan al mismo tiempo para detectar fallos en tanto en la red Nmos como Pmos del camino de conducción. El rango de detección para el caso de 2 señales mostró ser mayor que para el caso de una sola señal.

En el caso del **latch de compuertas de transmisión** se encuentra compuesto de las etapas: entrada, inversora (INV1, INV2) y de cierre de memoria. Se han considerado abiertos resistivos en las tres etapas. El retardo se incrementa

para abiertos resistivos en la etapa de entrada que afecten a ambos transistores de la compuerta de transmisión. El retardo se incrementa a medida que el valor del abierto resistivo también se incrementa. Por lo que un valor dado de R_{op} existe un valor de t_{xsu} critico para el cual se produce error lógico en el latch. Los abiertos resistivos que afectan a ambos transistores de la compuerta de tranmisión son semejantes al caso de abiertos resistivos de múltiple compuerta en el latch simétrico. Sin embargo si el abierto resistivo afecta solo a un transistor de la etapa de entrada entonces se observa un pequeño incremento de retardo debido a que el dato tiende a pasar por el transistor sin fallo, por lo que estos fallos serán de difícil detección. Los abiertos resistivos en la etapa inversora INV1 se comportan de manera muy parecida a los fallos en las etapas manejadoras y de salida del latch simétrico. Los fallos en la etapa inversora INV2 son afectados por efectos de redistribución de carga, a excepción del caso de múltiples compuertas. El impacto del efecto de redistribución de carga es que el segundo vector de pruebas puede ser invalidado por lo cual el defecto no se detecta. Abiertos resistivos en el camino de conducción en la etapa de cierre de memoria no son detectables por medio de prueba lógica o por prueba de retardo. Estos defectos son similares a aquellos en el camino de conducción de la etapa inversora con reloj del latch simétrico. Abiertos resistivos en el camino de control de la etapa de cierre de memoria son difíciles de detectar, solamente algunos casos bajo ciertas condiciones iniciales y grandes valores de abiertos resistivos son detectables. Algunos abiertos resistivos en el camino de conducción de la etapa de cierre de memoria pueden ser detectables si un circuito de DFT es utilizado. Tal circuito consiste en agregar un transistor Nmos manejado por una señal de control.

El **flip-flop simétrico** se encuentra formado por dos latches simétricos tipo D. Por lo que su análisis se puede dividir en: análisis en el latch maestro, análisis en el latch esclavo. Abiertos resistivos localizados en el latch maestro, a excepción de aquellos en la etapa de salida, se comportan de manera similar a los del caso del latch simétrico. La detección de estos es por medio de error lógico. Los casos de abiertos resistivos en la etapa de salida son influenciados por efectos de redistribución de carga. El impacto de la redistribución de carga es el de hacer más fácilmente detectable a los abiertos resistivos. Los abiertos resistivos en el latch

esclavo se pueden manifestar a la salida del flip-flop como error lógico y como retardos adicionales. La etapa manejadora del latch esclavo es idéntica a la etapa de entrada de un latch de compuertas de transmisión por lo que su comportamiento es similar. Mientras que los fallos localizados en la etapa inversora con reloj y de salida tienen un comportamiento similar a aquellas etapas en el latch simétrico.

De manera similar al flip-flop simetrico, el analisis en el **flip-flop de compuertas de transmisión** también se ha dividido en latch maestro y latch esclavo. Debido a la estructura identica de los latches maestro y esclavo, los casos de abiertos resistivos en el latch esclavo tienen un comportamiento similar al observado en un solo latch de compuertas de transmisión. Esto significa que los fallos son detectados por medio de prueba lógica o por medio de prueba de retardo. Para los fallo en el latch maestro, estos pueden ser detectados de manera similar al caso de un simple latch excepto los fallos que afectan al segundo inversor de la etapa inversora (INV2). Defectos localizados en el inversor INV2 son influenciados por un doble efecto de compartición de carga: una recarga y una descarga. El efecto combinado de la compartición de carga hace más fácil la detección del abierto resistivo.

El análisis en la **cadena scan path** se hizo considerando para flip-flops simétricos y de compuertas de transmisión como elementos componentes de la cadena. Todos los casos de abiertos resistivos se tomaron en un flip-flop interno. Solamente por medio de error lógico es posible determinar un abierto resistivo debido a que es necesario propagar el fallo a través de otros flip-flops. El comportamiento del flip-flop se dividió en bloques de acuerdo al tiempo en que el dato esta presente en el abierto resistivo en: abiertos resistivos antes de la señal de reloj, abiertos resistivos después de la señal de reloj y abiertos resistivos que producen error lógico en el siguiente latch.

Se obtuvieron condiciones de sincronización para que un error lógico apareciera a la salida de la cadena scan path como resultado de un abierto resistivo. El error lógico puede aparecer como consecuencia de dos posibles causas: violar el tiempo t_{xsu} del mismo flip-flop con fallo, violar las condiciones de sincronización del siguiente flip-flop sin fallo.

Para el caso de abiertos resistivos antes de la señal de reloj se requiere de un ciclo completo de reloj para escribir un dato, esto significa que estos casos son difíciles de detectar debido al tiempo del que se dispone. En cambio para abiertos resistivos después de la señal de reloj solo se dispone de medio ciclo de reloj por lo que estos abiertos resistivos son mas probables de detectar. Finalmente para el caso de abiertos resistivos que producen error lógico en el siguiente latch, se mostró que un reloj altamente asimétrico tiene mas probabilidades de detectar abiertos resistivos en una cadena scan path basada en flip-flops de compuertas de transmisión mientras que relojes no tan asimétricos son necesarios para cadenas scan path basadas en flip-flop simétricos.

Otro tema analizado fue el método de señales X-Y, el cual fue propuesto para detectar violaciones de retardo debido a señales rápidas basado en las regiones de operación de las zonas X-Y Cuando un sistema digital es caracterizado por su entrada y salida, en este caso llamadas X, Y, puede ser que su respuesta característica sea representada por medio de una gráfica de entrada y salida (gráfica X-Y). Dependiendo del retardo entre ambas señales, se tendrá una diferente figura en el plano X-Y desde una recta con pendiente positiva para el caso de señales en fase hasta una recta con pendiente negativa para el caso de señales en contrafase, pasando por una elipse con pendiente positiva en el caso de que ambas señales se encuentren desfasadas aproximadamente 45^o. La figura característica se repite con signo contrario para desfases mayores a 90^o. De tal manera que en un circuito en donde exista un incremento de retardo, se tendrá un curva X-Y mas semejante a un elipse. En este caso se hace uso de señales en contrafase, lo cual significa una línea recta con pendiente negativa. Sin embargo debido a los retardos en los sistemas digitales es difícil tener dos señales en perfecta contrafase por lo que la respuesta en el plano X-Y de un sistema sin retardo critico es una elipse con pendiente negativa. Para el caso de un sistema defectuoso, la curva X-Y será más ancha que un sistema no defectuoso, entonces es posible colocar líneas alrededor de la curva no defectuosa de manera que la encierren. Estas línea se les conoce como líneas de control y son definidas por la ecuación de la recta caracterizadas por su pendiente y ordenada en el origen. De esta forma se establece una zona dentro de las líneas de control y otra zona fuera de las líneas de

control. A cada zona (interna o externa) se le establece un valor lógico definido, esto significa que cualquier punto dentro de la zona interna representara un cero lógico, mientras que cualquier punto fuera de la zona interna representara un uno lógico. Al suceder una violación en los tiempos de retardo entonces la curva X-Y defectuosa cruzara las líneas de control por diferentes puntos, estas transiciones de zonas pueden ser contabilizadas en una firma digital.
Un posible circuito digital puede ser implementado por medio de un detector de subzonas, una compuerta OR y un contador asíncrono. El contador asíncrono es un contador digital convencional de 10 bits. El detector de subzona es formado por un detector X-Y y un comparador, de donde el detector X-Y realiza la línea de control. El detector X-Y se puede implementar por medio de los llamados dispositivos de compuerta flotante debido a que presentan características como que están basados en el concepto de compartición de carga en lugar de suma de corrientes, lo cual los hace tener una alta impedancia de entrada y ocupan muy pocos componentes para realizar una suma, de hecho son aditivos por naturaleza. Es por medio de la relación de capacitancias de entrada en el dispositivo de compuertas flotantes que se puede definir su región de operación
Como ejemplo de aplicación se mostró la detectabilidad de una señal bajo acoplo capacitivo. El acoplo capacitivo fue simulado por medio de un par de líneas agresoras (cadenas de inversores) afectando a una línea victima. Los resultados mostrarón que acoplos capacitivos de 90fF y mayores son detectables por medio de este circuito.

En conclusión se propuso un método orientado para la detección de violaciones de retardo para señales representadas en el plano X-Y, el cual consiste en encerrar la curva X-Y no defectuosa por medio de unas líneas de control, definiendo así un área interna y un área externa. A cada área se le define un nivel lógico por lo que si una curva (defectuosa) cruza el área definida por las líneas de control entonces se detecta el cruce. Cada línea de control puede ser definida por medio de su pendiente y su ordenada en el origen. El método propuesto puede ser implementado por medio de detectores de subzona con dispositivos de compuerta flotante.

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